

PERFORMANCE ANALYSIS OF CMOS COMPARATOR AND CNTFET COMPARATOR DESIGN

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Abstract

This paper presents an efficient, low power, fast-response Carbon NanoTube Field Effect Transistor (CNTFET) based comparator and shows the simulation results for the basic performance parameters for it. Due to the properties of Carbon Nanotube (CNT) the CNTFET devices show faster performance as compared to that of complementary metal oxide semiconductors (CMOS) devices. And hence CNTFET based comparator has to show much more improved performance compared to comparator design using CMOS. The performances such as delay, power and the transient results of the CNTFET comparator simulation are much more efficient. Both comparators are simulated in CADENCE.

Key Words: Carbon Nano-Tube Field Effect Transistor (CNTFET), MOSFET, CADENCE, Comparator, Delay and Power.

1. INTRODUCTION

Silicon based MOS Technology is the basic cell of today's Very Large Scale Integrated systems. Moore's law predicts that CMOS Technology has continued to scale down which has now reached to 32nm and latest 22nm nano-meter range scale [2]. And it is difficult to go further since the controlling parameters will be the problem. For these small dimensions the systems has to suffer from many non-ideal effects like as lowered trans-conductance, source to drain tunnelling, gate oxide leakage, reduction in ON state current, mismatch in devices, fluctuations in doping patterns, degradation of mobility, delay problems etc. Such non-ideal effects results to increase in short channel which will rise exponentially, high power density and several variations in process. Again as we go further scaling down the fabrication process parameters are difficult to control and also overall processing cost increases for scaled devices.

According to the prediction of the Industrial Technology Roadmap (ITR), in nano-ranges the density on the chip will be very high and will encounter some difficulties in terms of technology limitations.

In the device operation phenomenon, Schottky Barrier (SB) is one of the CNTFETs (as shown in Fig-1(a) and as shown in Fig-1(b)). Good DC current can be achieved by SB-controlled and performances for low power and high speed can be limited. Thus we shall see the alternatives for silicon transistors [3]. With the unique properties and if we could fabricate precisely, the next nano transistor generation design can be CNT based elements, which is CNTFETs. Near around from the year 2015(as per prediction of ITR) silicon will be replaced by new materials and their devices. The CNTs are also recognised as "wonder material" of new century. These are also referred as the basic building blocks

for silicon circuits [5]-[6]. CNTFET overcomes most of the basic limitations of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

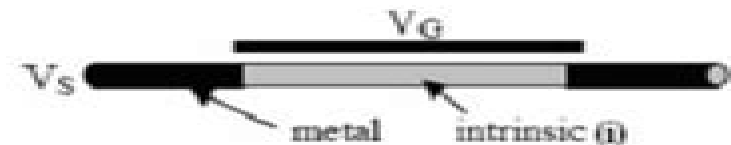


Fig -1(a): Schottky Barrier

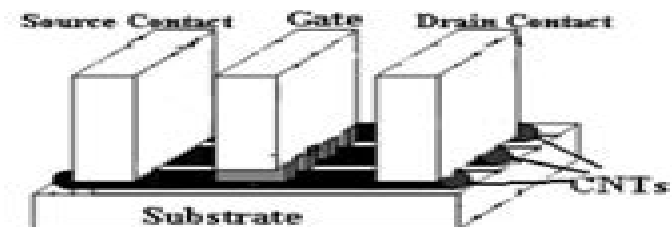


Fig -1(b): CNTFET

In this paper, section-2 describes the structure and characteristics of the device. Section-3 is presenting the design of classical comparator circuit and a new design. In section-4 performance parameters of CNTFET are compared with CMOS implementation. Finally section-5 concludes the paper.

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