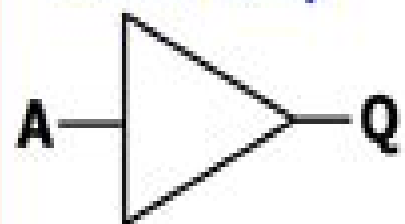
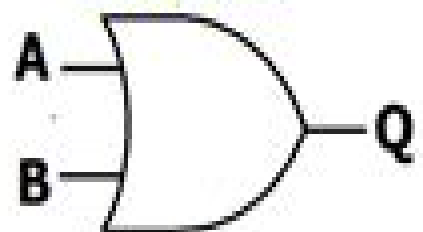


Buffer Amp



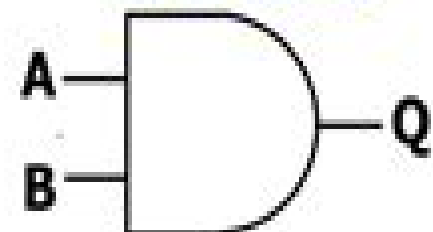
A	Q
0	0
1	1

OR Gate



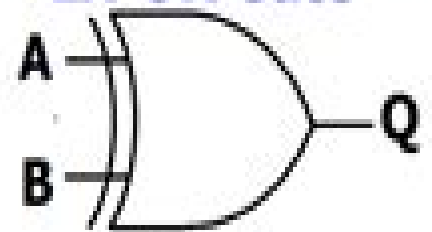
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

AND Gate



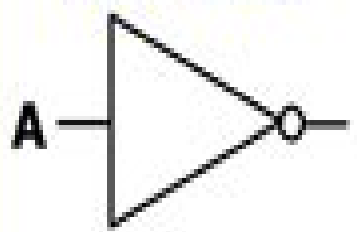
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

EX-OR Gate



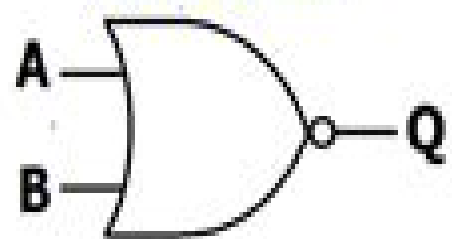
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

NOT Gate



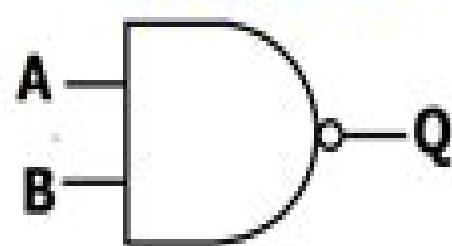
A	Q
0	1
1	0

NOR Gate



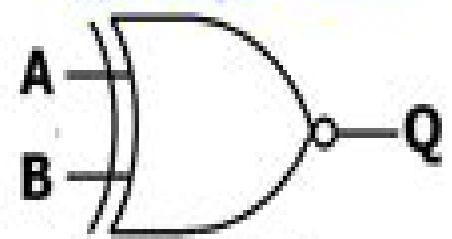
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

NAND Gate



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

EX-NOR Gate



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

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Chao Zhang



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