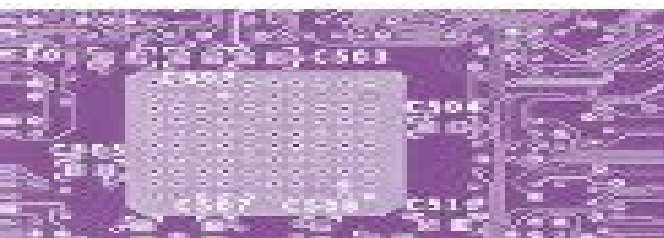




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ANALOG CIRCUITS AND DESIGN

STEVEN H. VOLDMAN



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Esd Analog Circuits And Design By Steven H Voldman

Steven H. Voldman



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ESD Steven H. Voldman, 2015-01-05 A comprehensive and in depth review of analog circuit layout schematic architecture device power network and ESD design This book will provide a balanced overview of analog circuit design layout analog circuit schematic development architecture of chips and ESD design It will start at an introductory level and will bring the reader right up to the state of the art Two critical design aspects for analog and power integrated circuits are combined The first design aspect covers analog circuit design techniques to achieve the desired circuit performance The second and main aspect presents the additional challenges associated with the design of adequate and effective ESD protection elements and schemes A comprehensive list of practical application examples is used to demonstrate the successful combination of both techniques and any potential design trade offs Chapter One looks at analog design discipline including layout and analog matching and analog layout design practices Chapter Two discusses analog design with circuits examining single transistor amplifiers multi transistor amplifiers active loads and more The third chapter covers analog design layout also MOSFET layout before Chapters Four and Five discuss analog design synthesis The next chapters introduce the reader to analog digital mixed signal design synthesis analog signal pin ESD networks and analog ESD power clamps Chapter Nine the last chapter covers ESD design in analog applications Clearly describes analog design fundamentals circuit fundamentals as well as outlining the various ESD implications Covers a large breadth of subjects and technologies such as CMOS LDMOS BCD SOI and thick body SOI Establishes an ESD analog design discipline that distinguishes itself from the alternative ESD digital design focus Focuses on circuit and circuit design applications Assessable with the artwork and tutorial style of the ESD book series PowerPoint slides are available for university faculty members Even in the world of digital circuits analog and power circuits are two very important but under addressed topics especially from the ESD aspect Dr Voldman s new book will serve as an essential and practical guide to the greater IC community With high practical and academic values this book is a bible for professionals graduate students device and circuit designers for investigating the physics of ESD and for product designs and testing

ESD Steven H. Voldman, 2006-02-03 The scaling of semiconductor devices from sub micron to nanometer dimensions is driving the need for understanding the design of electrostatic discharge ESD circuits and the response of these integrated circuits IC to ESD phenomena *ESD Circuits and Devices* provides a clear insight into the layout and design of circuitry for protection against electrical overstress EOS and ESD With an emphasis on examples this text explains ESD buffering ballasting current distribution design segmentation feedback coupling and de coupling ESD design methods outlines the fundamental analytical models and experimental results for the ESD design of MOSFETs and diode semiconductor device elements with a focus on CMOS silicon on insulator SOI and Silicon Germanium SiGe technology focuses on the ESD design optimization integration and synthesis of these elements and concepts into ESD networks as well as applying within the off chip driver networks and on chip receivers and highlights state of the art ESD input circuits as well

as ESD power clamps networks Continuing the author's series of books on ESD this book will be an invaluable reference for the professional semiconductor chip and system ESD engineer Semiconductor device and process development quality reliability and failure analysis engineers will also find it an essential tool In addition both senior undergraduate and graduate students in microelectronics and IC design will find its numerous examples useful *The ESD Handbook* Steven H. Voldman, 2021-04-12 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems **ESD** Steven H. Voldman, 2011-04-04 Electrostatic discharge ESD continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I/O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I/O guard rings ESD guard rings I/O to I/O and I/O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies discussed including CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS and smart power practical methods for the understanding of ESD circuit power distribution ground rule development internal bus distribution current path analysis

quality metrics ESD Design and Synthesis is a continuation of the author's series of books on ESD protection. It is an essential reference for ESD circuit and semiconductor engineers, design synthesis team leaders, layout design, characterisation, floorplanning, test and reliability engineers, technicians and groundrule and test site developers in the manufacturing and design of semiconductor chips. It is also useful for graduate and undergraduate students in electrical engineering, semiconductor sciences and manufacturing sciences and on courses involving the design of ESD devices, chips and systems. This book offers a useful insight into the issues that confront modern technology as we enter the nano electronic era. **ESD Basics** Steven H. Voldman, 2012-08-22 Electrostatic discharge ESD continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro to nano electronics. This book introduces the fundamentals of ESD, electrical overstress, EOS, electromagnetic interference, EMI, electromagnetic compatibility, EMC and latchup, as well as provides a coherent overview of the semiconductor manufacturing environment and the final system assembly. It provides an illuminating look into the integration of ESD protection networks followed by examples in specific technologies, circuits and chips. The text is unique in covering semiconductor chip manufacturing issues, ESD semiconductor chip design and system problems confronted today as well as the future of ESD phenomena and nano technology. Look inside for extensive coverage on: The fundamentals of electrostatics, triboelectric charging and how they relate to present day manufacturing environments of micro electronics to nano technology; Semiconductor manufacturing handling and auditing; processing to avoid ESD failures; ESD, EOS, EMI, EMC and latchup; semiconductor component and system level testing to demonstrate product resilience from human body model, HBM, transmission line pulse, TLP, charged device model, CDM, human metal model, HMM, cable discharge events, CDE to system level IEC 61000 4 2 tests; ESD on chip design and process; manufacturing practices and solutions to improve ESD; semiconductor chip solutions also practical off chip ESD protection and system level solutions to provide more robust systems. System level concerns in servers, laptops, disk drives, cell phones, digital cameras, hand held devices, automobiles and space applications. Examples of ESD design for state of the art technologies including CMOS, BiCMOS, SOI, bipolar technology, high voltage CMOS, HVCMOS, RF CMOS, smart power, magnetic recording technology, micro machines, MEMs to nano structures. **ESD Basics: From Semiconductor Manufacturing to Product Use** complements the author's series of books on ESD protection. For those new to the field, it is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic Era.

Integrated Circuit Design for Radiation Environments Stephen J. Gaul, Nicolaas van Vonno, Steven H. Voldman, Wesley H. Morris, 2019-12-31 A practical guide to the effects of radiation on semiconductor components of electronic systems and techniques for the designing, laying out and testing of hardened integrated circuits. This book teaches the fundamentals of radiation environments and their effects on electronic components as well as how to design, lay out and test cost effective hardened semiconductor chips not only for today's space systems but for commercial terrestrial applications as well. It

provides a historical perspective the fundamental science of radiation and the basics of semiconductors as well as radiation induced failure mechanisms in semiconductor chips Integrated Circuits Design for Radiation Environments starts by introducing readers to semiconductors and radiation environments including space atmospheric and terrestrial environments followed by circuit design and layout The book introduces radiation effects phenomena including single event effects total ionizing dose damage and displacement damage and shows how technological solutions can address both phenomena Describes the fundamentals of radiation environments and their effects on electronic components Teaches readers how to design lay out and test cost effective hardened semiconductor chips for space systems and commercial terrestrial applications Covers natural and man made radiation environments space systems and commercial terrestrial applications Provides up to date coverage of state of the art of radiation hardening technology in one concise volume Includes questions and answers for the reader to test their knowledge Integrated Circuits Design for Radiation Environments will appeal to researchers and product developers in the semiconductor space and defense industries as well as electronic engineers in the medical field The book is also helpful for system layout process device reliability applications ESD latchup and circuit design semiconductor engineers along with anyone involved in micro electronics used in harsh environments ESD Testing Steven H. Voldman, 2016-10-07 With the evolution of semiconductor technology and global diversification of the semiconductor business testing of semiconductor devices to systems for electrostatic discharge ESD and electrical overstress EOS has increased in importance ESD Testing From Components to Systems updates the reader in the new tests test models and techniques in the characterization of semiconductor components for ESD EOS and latchup Key features Provides understanding and knowledge of ESD models and specifications including human body model HBM machine model MM charged device model CDM charged board model CBM cable discharge events CDE human metal model HMM IEC 61000 4 2 and IEC 61000 4 5 Discusses new testing methodologies such as transmission line pulse TLP to very fast transmission line pulse VF TLP and future methods of long pulse TLP to ultra fast TLP UF TLP Describes both conventional testing and new testing techniques for both chip and system level evaluation Addresses EOS testing electromagnetic compatibility EMC scanning to current reconstruction methods Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing ESD Testing From Components to Systems is part of the authors series of books on electrostatic discharge ESD protection this book will be an invaluable reference for the professional semiconductor chip and system level ESD and EOS test engineer Semiconductor device and process development circuit designers quality reliability and failure analysis engineers will also find it an essential reference In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics semiconductor testing and experimental work *Electrical Overstress (EOS)* Steven H. Voldman, 2013-10-28 Electrical Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano

electronics This book teaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today's modern world Look inside for extensive coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e g such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000 4 2 test events EOS protection on chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author's series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano electronic era *Latchup* Steven H. Voldman, 2008-04-15 Interest in latchup is being renewed with the evolution of complementary metal oxide semiconductor CMOS technology metal oxide semiconductor field effect transistor MOSFET scaling and high level system on chip SOC integration Clear methodologies that grant protection from latchup with insight into the physics technology and circuit issues involved are in increasing demand This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena from basic over voltage and over current conditions single event latchup SEL and cable discharge events CDE to latchup domino phenomena It contains chapters focusing on bipolar physics latchup theory latchup and guard ring characterization structures characterization testing product level test systems product level testing and experimental results Discussions on state of the art semiconductor processes design layout and circuit level and system level latchup solutions are also included as well as latchup semiconductor process solutions for both CMOS to BiCMOS such as shallow trench deep trench retrograde wells connecting implants sub collectors heavily doped buried layers and buried grids from single to triple well CMOS practical latchup design methods automated and bench level latchup testing methods and techniques latchup theory of logarithm resistance space generalized alpha a space beta b space new latchup design methods connecting the

theoretical to the practical analysis and examples of latchup computer aided design CAD methodologies from design rule checking DRC and logical to physical design to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level Latchup acts as a companion text to the author s series of books on ESD electrostatic discharge protection serving as an invaluable reference for the professional semiconductor chip and system level ESD engineer Semiconductor device process and circuit designers and quality reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology Practitioners in the automotive and aerospace industries will also find it useful In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics computer aided design and design integration

Wireless Sensor Networks Jr., Edgar H. Callaway, 2003-08-26 Because they provide practical machine to machine communication at a very low cost the popularity of wireless sensor networks is expected to skyrocket in the next few years duplicating the recent explosion of wireless LANs *Wireless Sensor Networks Architectures and Protocols* describes how to build these networks from the layers of the

Electrostatic Discharge Steven Voldman, 2019-10-02 As we enter the nanoelectronics era electrostatic discharge ESD phenomena is an important issue for everything from micro electronics to nanostructures This book provides insight into the operation and design of micro gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies electrical breakdown in micro gaps nanogenerators from ESD and theoretical prediction and optimization of triboelectric nanogenerators The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design

IEEE International Reliability Physics Symposium Proceedings International Reliability Physics Symposium, 2004

The ESD Handbook Steven H. Voldman, 2021-03-02 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook

contains an accessible reference to ESD design and ESD systems **ESD** Steven H. Voldman, 2006-11-02 With the growth of high speed telecommunications and wireless technology it is becoming increasingly important for engineers to understand radio frequency RF applications and their sensitivity to electrostatic discharge ESD phenomena This enables the development of ESD design methods for RF technology leading to increased protection against electrical overstress EOS and ESD ESD RF Technology and Circuits Presents methods for co synthesizing ESD networks for RF applications to achieve improved performance and ESD protection of semiconductor chips discusses RF ESD design methods of capacitance load transformation matching network co synthesis capacitance shunts inductive shunts impedance isolation load cancellation methods distributed loads emitter degeneration buffering and ballasting examines ESD protection and design of active and passive elements in RF complementary metal oxide semiconductor CMOS RF laterally diffused metal oxide semiconductor LDMOS RF BiCMOS Silicon Germanium SiGe RF BiCMOS Silicon Germanium Carbon SiGeC and Gallium Arsenide technology gives information on RF ESD testing methodologies RF degradation effects and failure mechanisms for devices circuits and systems highlights RF ESD mixed signal design integration of digital analog and RF circuitry sets out examples of RF ESD design computer aided design methodologies covers state of the art RF ESD input circuits as well as voltage triggered to RC triggered ESD power clamps networks in RF technologies as well as off chip protection concepts Following the authors series of books on ESD this book will be a thorough overview of ESD in RF technology for RF semiconductor chip and ESD engineers Device and circuit engineers working in the RF domain and quality reliability and failure analysis engineers will also find it a valuable reference in the rapidly growing area of RF ESD design In addition it will appeal to graduate students in RF microwave technology and RF circuit design **Sci-tech News** ,2005 **ESD Basics** Steven H. Voldman, 2012-10-22 Electrostatic discharge ESD continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book introduces the fundamentals of ESD electrical overstress EOS electromagnetic interference EMI electromagnetic compatibility EMC and latchup as well as provides a coherent overview of the semiconductor manufacturing environment and the final system assembly It provides an illuminating look into the integration of ESD protection networks followed by examples in specific technologies circuits and chips The text is unique in covering semiconductor chip manufacturing issues ESD semiconductor chip design and system problems confronted today as well as the future of ESD phenomena and nano technology Look inside for extensive coverage on The fundamentals of electrostatics triboelectric charging and how they relate to present day manufacturing environments of micro electronics to nano technology Semiconductor manufacturing handling and auditing processing to avoid ESD failures ESD EOS EMI EMC and latchup semiconductor component and system level testing to demonstrate product resilience from human body model HBM transmission line pulse TLP charged device model CDM human metal model HMM cable discharge events CDE to system level IEC 61000 4 2 tests ESD on chip design and process manufacturing practices and solutions to improve ESD

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ESD Steven H. Voldman, 2004-10-29 This volume is the first in a series of three books addressing Electrostatic Discharge ESD physics devices circuits and design across the full range of integrated circuit technologies ESD Physics and Devices provides a concise treatment of the ESD phenomenon and the physics of devices operating under ESD conditions Voldman presents an accessible introduction to the field for engineers and researchers requiring a solid grounding in this important area The book contains advanced CMOS Silicon On Insulator Silicon Germanium and Silicon Germanium Carbon In addition it also addresses ESD in advanced CMOS with discussions on shallow trench isolation STI Copper and Low K materials Provides a clear understanding of ESD device physics and the fundamentals of ESD phenomena Analyses the behaviour of semiconductor devices under ESD conditions Addresses the growing awareness of the problems resulting from ESD phenomena in advanced integrated circuits Covers ESD testing failure criteria and scaling theory for CMOS SOI silicon on insulator BiCMOS and BiCMOS SiGe Silicon Germanium technologies for the first time Discusses the design and development implications of ESD in semiconductor technologies An invaluable reference for EMC non specialist engineers and researchers working in the fields of IC and transistor design Also suitable for researchers and advanced students in the fields of device circuit modelling and semiconductor reliability

IBM Journal of Research and Development ,2003 **ESD Design for Analog Circuits** Vladislav A. Vashchenko, Andrei Shibkov, 2010-07-27 This Book and Simulation Software Bundle Project Dear Reader this book project brings to you a unique study tool for ESD protection solutions used in analog integrated circuit IC design Quick start learning is combined with in depth understanding for the whole spectrum of cro disciplinary knowledge required to excel in the ESD eld The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies The book project provides two different options for learning the material The printed material can be studied as any regular technical textbook At the same time another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise The book is bundled with simpli ed trial version of commercial mixed TM mode simulation software from Angstrom Design Automation The DECIMM Device Circuit Mixed Mode simulator tool and complementary to the book s

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