

Digital Integrated Circuit Testing using Transient Signal Analysis

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Abstract

A novel approach to testing CMOS digital circuits is presented that is based on an analysis of I_{DD} switching transients on the supply rails and voltage transients at selected test points. We present simulation and hardware experiments which show distinguishable characteristics between the transient waveforms of defective and non-defective devices. These variations are shown to exist for CMOS open drain and bridging defects, located both on and off of a sensitized path.

1.0 Introduction

Transient Signal Analysis (TSA) is a new parametric testing method for digital integrated circuits. In TSA, transients in both the voltage waveforms at selected test points as well as current transients on the power supply are analyzed to determine the presence of defects. TSA exploits the fact that the power supply is globally connected to a large fraction of the transistors in a CMOS digital integrated circuit. TSA is similar to power supply current (I_{DD}) test methods in this way. Since power supply connections are unbuffered at the I/O pads, it is possible to measure the high frequency components of this signal without attenuation. Thus, the I_{DD} transients reflect the switching activity associated with the propagation of signals throughout the circuit. However, in larger circuits, the number of transistors which can simultaneously switch often makes it difficult to identify a defect using this single resource. TSA improves on defect detection capabilities of I_{DD} test strategies by additionally monitoring the voltage transients at a set of test points as well as on I_{DD} . The voltage test points are typically at or near the primary outputs of the device. By using a combination of voltage transients on test signal paths and I_{DD} transients on the power supply, TSA can provide improved defect resolution while maintaining a high degree of process insensitivity when compared with other I_{DD} -based testing methods.

In this paper, we present results from four experiments conducted on actual devices with intentionally inserted bridging and open drain defects. In order to demonstrate the sensitivity advantage of TSA over logic testing, we

have placed several bridging and open drain defects into separate versions of a test circuit and have conducted experiments using two-vector test sequences that do not generate logic errors at the test points. The results presented for the experiments show regional variations in the test point signals due to the presence of the defects.

The remainder of this paper is organized as follows. In Section 2 we present related research on device testing and the motivation for our research. Section 3 presents the results of hardware experiments conducted on devices with intentionally inserted bridging and open drain defects. Section 4 gives a summary and conclusions.

2.0 Background and Motivation

Device logic testing analyzes the logical integrity of the device by using input test vectors which are a subset of all possible stimuli. However, these subsets are generated by techniques which are based on fault models that have been shown to be inadequate to detect all forms of CMOS defects [1][2]. Parametric testing strategies [3][4], on the other hand, are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of supply current or transient response. While the algorithms for generating logic tests have been improved over time to handle more types of fault behaviors, parametric testing strategies offer intrinsically better solutions since they have been developed from the structural and electrical properties of CMOS circuits.

There are many types of parametric tests that have been proposed [5]. Recent research interest has focused primarily on three types: I_{DDQ} [6], I_{DD} [7], and delay fault testing [8][9]. I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value [10]. I_{DDQ} has been shown to be an effective diagnostic technique for CMOS bridging defects, but is of limited applicability for some types of CMOS open defects [11]. Although defect observability is significantly improved by the addition of I_{DDQ} to logic tests, I_{DDQ} is handicapped by the necessarily slow test vector application rates, the limited resolution achievable for large ICs and the restricted class of CMOS circuits to which it is applicable.

Several dynamic supply current I_{DD} -based approaches

Digital Integrated Circuit Testing Using Transient Signal

John D. Cressler, H. Alan Mantooth



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VLSI Testing Stanley Leonard Hurst, 1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course on the subject Annotation copyrighted by Book News Inc Portland OR *Integrated Circuits* Peter Shepherd, 1996-11-11 Integrated circuits have revolutionised the world of electronics and the associated areas of computing and communication In past years the tasks of designing manufacturing and testing these types of circuit were restricted to a few specialist engineers However within recent years the proliferation of computer tools and affordable access to IC manufacturing foundries has resulted in a substantial increase in the number of people designing ICs for the first time both in universities and colleges and in industry This book introduces the reader to all aspects of IC design manufacture and testing with a minimum of mathematics but with relevant examples at each stage It examines the overall design strategies the engineering trade offs and the advantages disadvantages and optimum applications of each available technology **IC Test Using the Energy Consumption Ratio** Wanli Jiang, 2000 *Fault Diagnosis of Analog Integrated Circuits* Prithviraj Kabisatpathy, Alok Barua, Satyabroto Sinha, 2006-01-13 System on Chip SOC having both digital and analog circuits has become increasingly prevalent in integrated circuit manufacturing industry Electronic tests are classified as digital analog and mixed signal Current methodologies for the testing of digital circuits are well developed In contrast methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals Compared to digital testing analog testing lags far behind in methodologies and tools and therefore demands substantial research and development effort Fault Diagnosis of Analog Integrated Circuits is a textbook for advanced undergraduate and graduate level students as well as practicing engineers The objective of this book is to study the testing and fault diagnosis of analog and analog part of mixed signal circuits A background in analog integrated circuit artificial neural network is desirable but not essential The text covers the testing and fault diagnosis of both bipolar and Metal Oxide Semiconductor MOS circuits Fault model of the devices in analog domain has been introduced in the text The test stimulus generations are also discussed in details Experimental verification of some state of the art techniques has also been presented in the book It also contains problems that can be used as quiz or homework This book enables the reader to test an analog circuit that is implemented either in bipolar or MOS technology **DCIS2002** Salvador Bracho del Pino, Mar Martínez, Teresa Riesgo, Miguel Ángel Allende Recio, 2002 Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena Santander en noviembre de 2002 Esta Conferencia ha alcanzado un alto

nivel de calidad como consecuencia de su tradición y madurez que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa. Desde su origen tiene una gran contribución de Universidades españolas aunque hoy los autores participan desde catorce países.

VLSI: Integrated Systems on Silicon Ricardo A. Reis, Luc Claesen, 2013-06-05 This book contains the papers that have been presented at the ninth Very Large Scale Integrated Systems conference VLSI 97 that is organized biannually by IFIP Working Group 10.5. It took place at Hotel Serra Azul in Gramado, Brazil from 26-30 August 1997. Previous conferences have taken place in Edinburgh, Trondheim, Vancouver, Munich, Grenoble and Tokyo. The papers in this book report on all aspects of importance to the design of the current and future integrated systems. The current trend towards the realization of versatile Systems on a Chip requires attention of embedded hardware, software, systems, dedicated ASIC hardware, sensors and actuators, mixed analog/digital design, video and image processing, low power, battery operation and wireless communication. The papers as presented in this book have been organized in two tracks where one is dealing with VLSI System Design and Applications and the other presents VLSI Design Methods and CAD. The following topics are addressed: VLSI System Design and Applications Track; VLSI for Video and Image Processing; Microsystem and Mixed mode design; Communication and Memory System Design; Core voltage; Low power Analog Circuits; High Speed Circuit Techniques; Application Specific DSP Architectures; VLSI Design Methods and CAD Track; Specification and Simulation at System Level; Synthesis and Technology Mapping; CAD Techniques for Low Power Design; Physical Design Issues in Sub-micron Technologies; Architectural Design and Synthesis; Testing in Complex Mixed Analog and Digital Systems.

18th IEEE VLSI Test Symposium, 2000. Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems. Themes are: microprocessor test validation; low power BIST and scan technology trends; scan related approaches; defect driven techniques; and system on chip test techniques. Other subjects are: analog test techniques; temperature and process drift issues; test compaction and design validation; analog BIST and functional test and verification issues. Also covered are: STIL extension; IDDQ test and on line testing and fault tolerance. Lacks a subject index. Annotation copyrighted by Book News, Inc., Portland, OR.

Electronic Design Automation for IC System Design, Verification, and Testing Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition. Electronic Design Automation for IC System Design, Verification and Testing thoroughly examines system level design, microarchitectural design, logic verification and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit (IC) designs; design and verification languages; digital simulation; hardware acceleration and emulation; and much more. New to This Edition: Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE).

costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **IEEE VLSI Test Symposium** ,2004 *Proceedings* ,2002 **Proceedings, International Test Conference 1996** ,1996 ITC is the World s largest premier technical conference on the testing and total quality of integrated electronics and the assemblies and systems that are based on them **19th IEEE VLSI Test Symposium** ,2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices* Ronald Donald Schrimpf,Dan M. Fleetwood,2004 This book provides a detailed treatment of radiation effects in electronic devices including effects at the material device and circuit levels The emphasis is on transient effects caused by single ionizing particles single event effects and soft errors and effects produced by the cumulative energy deposited by the radiation total ionizing dose effects Bipolar Si and SiGe metal oxide semiconductor MOS and compound semi conductor technologies are discussed In addition to considering the specific issues associated with high performance devices and technologies the book includes the background material necessary for understanding radiation effects at a more general level **Official Gazette of the United States Patent and Trademark Office** United States. Patent and Trademark Office,2002 *Scientific and Technical Aerospace Reports* ,1994 *Proceedings Ieee*,2004 The proceedings of the 21st IEEE VLSI test symposium VTS 2003 describing innovations in the testing of integrated circuits and systems

Curriculum Handbook with General Information Concerning ... for the United States Air Force Academy United States Air Force Academy,198? **Lecture Notes in Analog Electronics** Vančo B. Litovski,2025-01-17 Prof Van o Litovski was born in 1947 in Rakita South Macedonia Greece He graduated from the Faculty of Electronic Engineering in Ni in 1970 and obtained his M Sc in 1974 and his Ph D in 1977 He was appointed as a teaching assistant at the Faculty of

Electronic Engineering in 1970 and became a full professor at the same faculty in 1987 He was elected as a visiting professor honoris causa at the University of Southampton in 1999 From 1987 until 1990 he was a consultant to the CEO of Ei and was the head of the Chair of Electronics at the Faculty of Electronic Engineering in Ni for 12 years From 2015 to 2017 he was a researcher at the University of Bath He received several awards including from the Faculty of Electronic Engineering Charter in 1980 Charter in 1985 and a Special Recognition in 1995 and the University of Ni Plaque 1985 **Energy Research Abstracts** ,1992-10 *Extreme Environment Electronics* John D. Cressler,H. Alan Mantooth,2017-12-19

Unfriendly to conventional electronic devices circuits and systems extreme environments represent a serious challenge to designers and mission architects The first truly comprehensive guide to this specialized field Extreme Environment Electronics explains the essential aspects of designing and using devices circuits and electronic systems intended to operate in extreme environments including across wide temperature ranges and in radiation intense scenarios such as space The Definitive Guide to Extreme Environment Electronics Featuring contributions by some of the world s foremost experts in extreme environment electronics the book provides in depth information on a wide array of topics It begins by describing the extreme conditions and then delves into a description of suitable semiconductor technologies and the modeling of devices within those technologies It also discusses reliability issues and failure mechanisms that readers need to be aware of as well as best practices for the design of these electronics Continuing beyond just the paper design of building blocks the book rounds out coverage of the design realization process with verification techniques and chapters on electronic packaging for extreme environments The final set of chapters describes actual chip level designs for applications in energy and space exploration Requiring only a basic background in electronics the book combines theoretical and practical aspects in each self contained chapter Appendices supply additional background material With its broad coverage and depth and the expertise of the contributing authors this is an invaluable reference for engineers scientists and technical managers as well as researchers and graduate students A hands on resource it explores what is required to successfully operate electronics in the most demanding conditions

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- This book is crafted in an easy-to-understand language and is complemented by engaging illustrations. This book is highly recommended for anyone seeking to gain a comprehensive understanding of Digital Integrated Circuit Testing Using Transient Signal.

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