






Circuit Diagram and Truth Table

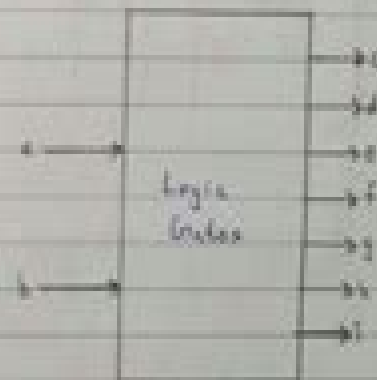
Type	Symbol	Boolean Algebra using A & B	Truth Table		
			INPUTS		OUTPUT
AND		$A \cdot B$	A	B	A AND B
			0	0	0
			0	1	0
			1	0	0
			1	1	1
OR		$A + B$	INPUTS		OUTPUT
			A	B	A OR B
			0	0	0
			0	1	1
			1	0	1
			1	1	1
NOT		\bar{A}	INPUTS		OUTPUT
			A		A'
			0		1
NAND		$\overline{A \cdot B}$	INPUTS		OUTPUT
			A	B	A NAND B
			0	0	1
			0	1	1
			1	0	1
			1	1	0
NOR		$\overline{A + B}$	INPUTS		OUTPUT
			A	B	A NOR B
			0	0	1
			0	1	0
			1	0	0
			1	1	0

Realization of Logic Gates and Familiarization of Verilog

AIM:

To implement logic gates using verilog.

Block Diagram:



TRUTH TABLE:

A	B	C	D	E	F	G	H	I
0	0	0	0	1	1	1	0	1
0	1	0	1	1	1	0	1	0
1	0	0	1	0	1	0	1	0
1	1	1	1	0	0	0	0	1

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