

***EE 671: VLSI DESIGN COURSE
for
Master and Bachelor Class of 2010***

Logical Effort- A Way of Designing Fast CMOS Circuits

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Logical Effort Ivan Sutherland, Robert F. Sproull, David Harris, 1999 Designers of high speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets Logical Effort Designing Fast CMOS Circuits makes high speed design easier and more methodical providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology capacitance and gate sizes The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull logical effort will change the way you approach design challenges This book begins by equipping you with a sound understanding of the method s essential procedures and concepts so you can start using it immediately Later chapters explore the theory and finer points of the method and detail its specialized applications Features Explains the method and how to apply it in two practically focused chapters Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions Offers easy ways to choose the fastest circuit from among an array of potential circuit designs Reduces the time spent on tweaking and simulations so you can rapidly settle on a good design Offers in depth coverage of specialized areas of application for logical effort skewed or unbalanced gates other circuit families including pseudo NMOS and domino wide structures such as decoders and irregularly forking circuits Presents a complete derivation of the method so you see how and why it works

CMOS Processors and Memories Krzysztof Iniewski, 2010-08-09 CMOS Processors and Memories addresses the state of the art in integrated circuit design in the context of emerging computing systems New design opportunities in memories and processor are discussed Emerging materials that can take system performance beyond standard CMOS like carbon nanotubes graphene ferroelectrics and tunnel junctions are explored CMOS Processors and Memories is divided into two parts processors and memories In the first part we start with high performance low power processor design followed by a chapter on multi core processing They both represent state of the art concepts in current computing industry The third chapter deals with asynchronous design that still carries lots of promise for future computing needs At the end we present a hardware design space exploration methodology for implementing and analyzing the hardware for the Bayesian inference framework This particular methodology involves analyzing the computational cost and exploring candidate hardware components proposing various custom architectures using both traditional CMOS and hybrid nanotechnology CMOL The first part concludes with hybrid CMOS Nano architectures The second memory part covers state of the art SRAM DRAM and flash memories as well as emerging device concepts Semiconductor memory is a good example of the full custom design that applies various analog and logic circuits to utilize the memory cell s device physics Critical physical effects that include tunneling hot electron injection charge trapping Flash memory are discussed in detail Emerging memories like FRAM PRAM and ReRAM that depend on magnetization electron spin alignment ferroelectric effect built in potential well quantum effects and thermal melting are also described CMOS Processors and Memories is a must for anyone serious about circuit design for

future computing technologies The book is written by top notch international experts in industry and academia It can be used in graduate course curriculum

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