SE-SEMITE CEXTC) (Rev) may 2013 D. L. D. - 2015/13

108: 1ST HALF-13 (r)-JP

Con. 6524-13.

GS-6336
(3 Hours) [Total Marks : 100

7

8

5

- N.B. (1) Question No. 1 is compulsory.
 - (2) Attempt any four from remaining questions.
 - (3) Figures to the right indicate full marks.
- 1. (a) Give TTL-CMOS interfacing.
 - (b) Compare combinational circuit with sequential circuit.

 (c) Compare binary code with BCD code. Give the example.

 5
 - (d) Compare synchronous with asynchronous counter. 5
- (a) Using Quine McClusky technique, minimize the following function:— 10
 F(A, B, C, D) = ∑m (3, 4, 5, 7, 9, 13, 14, 15)
 - (b) Design a 2 bit synchronous up/down counter using T-flip flops.
- (a) Implement the following Boolean function using single 4: 1 MUX and few logic 10 gates:—
 - $F(A, B, C, D) = \sum m(0, 2, 4, 5, 7, 8, 9, 11, 14)$ (b) Compare the various logic families with respect to their characteristics. Give at 10
 - least five points with their practical values.
- 4. (a) Draw and explain the working of Universal Shift Register.
 - (b) Design a circuit to compare two 2-bit numbers. Implement this circuit using only 10 NOR gates.
- 5. (a) Using one's and two's compliment methods perform (52)₁₀ (18)₁₀. 5
 - (b) Using Boolean Laws prove that:—

 ABC + ABC + ABC + ABC = AB + BC + CA
 - (c) Design BCD to Excess 3 code coverter. 10
- (a) Draw a neat circuit of master slave JK flip flop using logic gates. Write its truth 10 table and explain its operation.
 - (b) Draw a neat circuit of BCD adder and explain its working.
- 7. Write short notes on the following :-
 - (a) One bit comparator
 - (b) FPGA

(c) Fan in and Fan out.

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