Digital Integrated Circuits

A DESIGN PERSPECTIVE
SECOND EDITION



JAN M. RABAEY ANANTHA CHANDRAKASAN BORIVOJE NIKOLIC

Digital Integrated Circuits 2nd Edition

John P. Uyemura

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delves into the dramatic advances in the field including new applications and changes in the physics of operation made possible by relentless miniaturization This book was conceived in the versatile spirit of the field to bridge a void that had existed between books on transistor electronics and those covering VLSI design and fabrication as a separate topic Like the first edition this volume is a crucial link for integrated circuit engineers and those studying the field supplying the cross disciplinary connections they require for guidance in more advanced work For pedagogical reasons the author uses SPICE level 1 computer simulation models but introduces BSIM models that are indispensable for VLSI design This enables users to develop a strong and intuitive sense of device and circuit design by drawing direct connections between the hand analysis and the SPICE models With four new chapters more than 200 new illustrations numerous worked examples case studies and support provided on a dynamic website this text significantly expands concepts presented in the first edition Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor Embedded SoPC Design with Nios II Processor and Verilog Examples takes a learn by doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board Emphasizing hardware design and integration throughout the book is divided into four major parts Part I covers HDL and synthesis of custom hardware Part II introduces the Nios II processor and provides an overview of embedded software development Part III demonstrates the design and development of hardware and software of several complex I O peripherals including a PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides several case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology While designing and developing an embedded SoPC can be rewarding the learning can be a long and winding journey This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology Space Microelectronics Volume 2: Integrated Circuit Design for Space Applications Anatoly Belous, Vitali Saladukha, Siarhei Shvedau, 2017-07-31 This invaluable second volume of a two volume set is filled with details about the integrated circuit design for space applications Various considerations for the selection and application of electronic components for designing spacecraft are discussed The basic constructions of submicron transistors and

schottky diodes during the technological process of production are explored This book provides details on the energy consumption minimization methods for microelectronic devices Specific topics include Features and physical mechanisms of the effect of space radiation on all the main classes of microcircuits including peculiarities of radiation impact on submicron integrated circuits Special design technology and schematic methods of increasing the resistance to various types of space radiation Recommendations for choosing research equipment and methods for irradiating various samples Microcircuit designers on the composition of test elements for the study of the effect of radiation Microprocessors circuit boards logic microcircuits digital analog digital analog microcircuits manufactured in various technologies bipolar CMOS BiCMOS SOI Problems involved with designing high speed microelectronic devices and systems based on SOS and SOI structures System on chip and system in package and methods for rejection of silicon microcircuits with hidden defects during mass production

<u>Digital Integrated Circuits</u> John E. Ayers, 2018-09-03 Exponential improvement in functionality and performance of digital integrated circuits has revolutionized the way we live and work The continued scaling down of MOS transistors has broadened the scope of use for circuit technology to the point that texts on the topic are generally lacking after a few years The second edition of Digital Integrated Circuits Analysis and Design focuses on timeless principles with a modern interdisciplinary view that will serve integrated circuits engineers from all disciplines for years to come Providing a revised instructional reference for engineers involved with Very Large Scale Integrated Circuit design and fabrication this book delves into the dramatic advances in the field including new applications and changes in the physics of operation made possible by relentless miniaturization This book was conceived in the versatile spirit of the field to bridge a void that had existed between books on transistor electronics and those covering VLSI design and fabrication as a separate topic Like the first edition this volume is a crucial link for integrated circuit engineers and those studying the field supplying the cross disciplinary connections they require for guidance in more advanced work For pedagogical reasons the author uses SPICE level 1 computer simulation models but introduces BSIM models that are indispensable for VLSI design This enables users to develop a strong and intuitive sense of device and circuit design by drawing direct connections between the hand analysis and the SPICE models With four new chapters more than 200 new illustrations numerous worked examples case studies and support provided on a dynamic website this text significantly expands concepts presented in the first edition Electronic Design Automation Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng, 2009-03-11 This book provides broad and comprehensive coverage of the entire EDA flow EDA VLSI practitioners and researchers in need of fluency in an adjacent field will find this an invaluable reference to the basic EDA concepts principles data structures algorithms and architectures for the design verification and test of VLSI circuits Anyone who needs to learn the concepts principles data structures algorithms and architectures of the EDA flow will benefit from this book Covers complete spectrum of the EDA flow from ESL design modeling to logic test synthesis verification physical design and test helps EDA newcomers to get up and running

quickly Includes comprehensive coverage of EDA concepts principles data structures algorithms and architectures helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books including Test compression ESL design modeling large scale floorplanning placement routing synthesis of clock and power ground networks helps readers to design develop testable chips or products Includes industry best practices wherever appropriate in most chapters helps readers avoid costly mistakes **Fundamentals Of Solid State Electronics** Chih Tang Sah, 1991-10-30 This is perhaps the most comprehensive undergraduate textbook on the fundamental aspects of solid state electronics It presents basic and state of the art topics on materials physics device physics and basic circuit building blocks not covered by existing textbooks on the subject Each topic is introduced with a historical background and motivations of device invention and circuit evolution Fundamental physics is rigorously discussed with minimum need of tedious algebra and advanced mathematics Another special feature is a systematic classification of fundamental mechanisms not found even in advanced texts It bridges the gap between solid state device physics covered here with what students have learnt in their first two years of study Used very successfully in a one semester introductory core course for electrical and other engineering materials science and physics junior students the second part of each chapter is also used in an advanced undergraduate course on solid state devices The inclusion of previously unavailable analyses of the basic transistor digital circuit building blocks and cells makes this an excellent reference for engineers to look up fundamental concepts and data design formulae and latest devices such as the GeSi heterostructure bipolar transistors Circuit Design for CMOS VLSI John P. Uyemura, 2012-12-06 During the last decade CMOS has become increasingly attractive as a basic integrated circuit technology due to its low power at moderate frequencies good scalability and rail to rail operation. There are now a variety of CMOS circuit styles some based on static complementary con ductance properties but others borrowing from earlier NMOS techniques and the advantages of using clocking disciplines for precharge evaluate se quencing In this comprehensive book the reader is led systematically through the entire range of CMOS circuit design Starting with the in dividual MOSFET basic circuit building blocks are described leading to a broad view of both combinatorial and sequential circuits Once these circuits are considered in the light of CMOS process technologies important topics in circuit performance are considered including characteristics of interconnect gate delay device sizing and I O buffering Basic circuits are then composed to form macro elements such as multipliers where the reader acquires a unified view of architectural performance through par allelism and circuit performance through careful attention to circuit level and layout design optimization Topics in analog circuit design reflect the growing tendency for both analog and digital circuit forms to be combined on the same chip and a careful treatment of BiCMOS forms introduces the reader to the combination of both FET and bipolar technologies on the same chip to provide improved performance Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications Yosi Shacham-Diamand, Tetsuya Osaka, Madhav Datta, Takayuki Ohba, 2009-09-19 In Advanced ULSI interconnects fundamentals

and applications we bring a comprehensive description of copper based interconnect technology for ultra lar scale integration ULSI technology for integrated circuit IC application In grated circuit technology is the base for all modern electronics systems You can not electronics systems today everywhere from toys and home appliances to a planes and space shuttles Electronics systems form the hardware that together with software are the bases of the modern information society The rapid growth and vast exploitation of modern electronics system create a strong demand for new and improved electronic circuits as demonstrated by the amazing progress in the eld of ULSI technology This progress is well described by the famous Moore's law which states in its most general form that all the metrics that describe integrated circuit performance e g speed number of devices chip area improve expon tially as a function of time For example the number of components per chip d bles every 18 months and the critical dimension on a chip has shrunk by 50% every 2 years on average in the last 30 years This rapid growth in integrated circuits te nology results in highly complex integrated circuits with an increasing number of interconnects on chips and between the chip and its package The complexity of the interconnect network on chips involves an increasing number of metal lines per interconnect level more interconnect levels and at the same time a reduction in the interconnect line critical dimensions Design of High-Speed Time-Interleaved Delta-Sigma D/A Converters Ameya Bhide, 2015-08-19 Digital to analog D A converters or DACs are one the fundamental building blocks of wireless transmitters In order to support the increasing demand for highdata ate communication a large bandwidth is required from the DAC With the advances in CMOS scaling there is an increasing trend of moving a large part of the transceiver functionality to the digital domain in order to reduce the analog complexity and allow easy reconguration for multiple radio standards DACs can t very well into this trend of digital architectures as they contain a large digital signal processing component and oer two advantages over the traditionally used Nyquist DACs Firstly the number of DAC unit current cells is reduced which relaxes their matching and output impedance requirements and secondly the reconstruction lter order is reduced Achieving a large bandwidth from DACs requires a very high operating frequency of many GHz from the digital blocks due to the oversampling involved This can be very challenging to achieve using conventional DAC architectures even in nanometer CMOS processes Time interleaved TIDSM DACs have the potential of improving the bandwidth and sampling rate by relaxing the speed of the individual channels However they have received only some attention over the past decade and very few previous works been reported on this topic Hence the aim of this dissertation is to investigate architectural and circuit techniques that can further enhance the bandwidth and sampling rate of TIDSM DACs The rst work is an 8 GS s interleaved DAC prototype IC with 200 MHz bandwidth implemented in 65 nm CMOS The high sampling rate is achieved by a two channel interleaved MASH 1 1 digital modulator with 3 bit output resulting in a highly digital DAC with only seven current cells Two channel interleaving allows the use of a single clock for both the logic and the nal multiplexing This requires each channel to operate at half the sampling rate i e 4 GHz This is enabled by a high speed pipelined MASH

structure with robust static logic Measurement results from the prototype show that the DAC achieves 200 MHz bandwidth 57 dBc IM3 and 26 dB SNDR with a power consumption of 68 mW at 1 V digital and 1 2 V analog supplies This architecture shows good potential for use in the transmitter baseband While a good linearity is obtained from this DAC the SNDR is found to be limited by the testing setup for sending high speed digital data into the prototype The performance of a two channel interleaved DAC is found to be very sensitive to the duty cycle of the half rate clock The second work analyzes this eect mathematically and presents a new closed form expression for the SNDR loss of two channel DACs due to the duty cycle error DCE for a noise transfer function NTF of 1 z 1 n It is shown that a low order FIR lter after the modulator helps to mitigate this problem A closed form expression for the SNDR loss in the presence of this lter is also developed These expressions are useful for choosing a suitable modulator and lter order for an interleaved DAC in the early stage of the design process A comparison between the FIR lter and compensation techniques for DCE mitigation is also presented The nal work is a 11 GS s 1 1 GHz bandwidth time interleaved DAC prototype IC in 65 nm CMOS for the 60 GHz radio baseband The high sampling rate is again achieved by using a two channel interleaved MASH 1 1 architecture with a 4 bit output i e only fteen analog current cells The single clock architecture for the logic and the multiplexing requires each channel to operate at 5 5 GHz To enable this a new look ahead technique is proposed that decouples the two channels within the modulator feedback path thereby improving the speed as compared to conventional loop unrolling Full speed DAC testing is enabled by an on chip 1 Kb memory whose read path also operates at 5 5 GHz Measurement results from the prototype show that the DAC achieves 53 dB SFDR 49 dBc IM3 and 39 dB SNDR within a 1 1 GHz bandwidth while consuming 117 mW from 1 V digital 1 2 V analog supplies The proposed DAC can satisfy the spectral mask of the 60 GHz radio IEEE 802 11ad WiGig standard with a second order reconstruction lter Introduction to VLSI Systems Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding Millimeter-Wave Integrated Circuits Eoin Carey, Sverre Lidholm, 2005-12-05 Millimeter Wave Integrated Circuits delivers a detailed overview of MMIC design specifically focusing on designs for the millimeter wave mm wave frequency range The scope of the book is broad spanning detailed discussions of high frequency materials and technologies high frequency devices and the design of high frequency circuits The design material is supplemented as appropriate by theoretical analyses The broad scope of the book gives the reader a good theoretical and practical understanding of mm wave circuit design It is best suited for both undergraduate students who are reading or studying high frequency circuit design and postgraduate students who are specializing in the mm wave field FPGA Prototyping by SystemVerilog Examples Pong P. Chu, 2018-05-04 A hands on introduction to FPGA prototyping and SoC design This is the successor edition of the popular FPGA Prototyping by Verilog

Examples text It follows the same learning by doing approach to teach the fundamentals and practices of HDL synthesis and FPGA prototyping The new edition uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP intellectual property cores integrate them into an SoC system on a chip framework realize the system on an FPGA prototyping board and verify the hardware and software operation. The examples start with simple gate level circuits progress gradually through the RT register transfer level modules and lead to a functional embedded system with custom I O peripherals and hardware accelerators Although it is an introductory text the examples are developed in a rigorous manner and the derivations follow the strict design guidelines and coding practices used for large complex digital systems The book is completely updated and uses the SystemVerilog language which absorbs the Verilog language It presents the hardware design in the SoC context and introduces the hardware software co design concept Instead of treating examples as isolated entities the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software programmability and develop complex and interesting embedded system projects The new edition Adds four general purpose IP cores which are multi channel PWM pulse width modulation controller I2C controller SPI controller and XADC Xilinx analog to digital converter controller Introduces a music synthesizer constructed with a DDFS direct digital frequency synthesis module and an ADSR attack decay sustain release envelope generator Expands the original video controller into a complete stream based video subsystem that incorporates a video synchronization circuit a test pattern generator an OSD on screen display controller a sprite generator and a frame buffer Provides a detailed discussion on blocking and nonblocking statements and coding styles Describes basic concepts of software hardware co design with Xilinx MicroBlaze MCS soft core processor Provides an overview of bus interconnect and interface circuit Presents basic embedded system software development Suggests additional modules and peripherals for interesting and challenging projects FPGA Prototyping by SystemVerilog Examples makes a natural companion text for introductory and advanced digital design courses and embedded system courses It also serves as an ideal self teaching guide for practicing engineers who wish to learn more about this emerging area of interest Handbook of Signal Processing Systems Shuvra S. Bhattacharyya, Ed F. Deprettere, Rainer Leupers, Jarmo Takala, 2010-09-10 It gives me immense pleasure to introduce this timely handbook to the research velopment communities in the eld of signal processing systems SPS This is the rst of its kind and represents state of the arts coverage of research in this eld The driving force behind information technologies IT hinges critically upon the major advances in both component integration and system integration The major breakthrough for the former is undoubtedly the invention of IC in the 50 s by Jack S Kilby the Nobel Prize Laureate in Physics 2000 In an integrated circuit all components were made of the same semiconductor material Beginning with the pocket calculator in 1964 there have been many increasingly complex applications followed In fact processing gates and memory storage on a chip have since then grown at an exponential rate following Moore s Law Moore himself admitted that Moore s Law had turned out to be more

accurate longer lasting and deeper in impact than he ever imagined With greater device integration various signal processing systems have been realized for many killer IT applications Further breakthroughs in computer sciences and Internet technologies have also catalyzed large scale system integration All these have led to today s IT revolution which has profound impacts on our lifestyle and overall prospect of humanity It is hard to imagine life today without mobiles or Internets The success of SPS requires a well concerted integrated approach from mul ple disciplines such as device design Handbook of Integrated Circuit Industry Yangyuan Wang, Min-Hwa Chi, Jesse Jen-Chung Lou, Chun-Zhang Chen, 2023-11-27 Written by hundreds experts who have made contributions to both enterprise and academics research these excellent reference books provide all necessary knowledge of the whole industrial chain of integrated circuits and cover topics related to the technology evolution trends fabrication applications new materials equipment economy investment and industrial developments of integrated circuits Especially the coverage is broad in scope and deep enough for all kind of readers being interested in integrated circuit industry Remarkable data collection update marketing evaluation enough working knowledge of integrated circuit fabrication clear and accessible category of integrated circuit products and good equipment insight explanation etc can make general readers build up a clear overview about the whole integrated circuit industry This encyclopedia is designed as a reference book for scientists and engineers actively involved in integrated circuit research and development field In addition this book provides enough guide lines and knowledges to benefit enterprisers being interested in integrated circuit industry Noise Contamination in Nanoscale VLSI Circuits Selahattin Sayil, 2022-08-31 This textbook provides readers with a comprehensive introduction to various noise sources that significantly reduce performance and reliability in nanometer scale integrated circuits The author covers different types of noise such as crosstalk noise caused by signal switching of adjacent wires power supply noise or IR voltage drop in the power line due to simultaneous buffer gate switching events substrate coupling noise radiation induced transients thermally induced noise and noise due to process and environmental Coverages also includes the relationship between some of these noise sources as well as compound effects and modeling and mitigation of noise mechanisms **Integrated Circuit** and System Design Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-09-07 This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation

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