

PRACTICAL LOW POWER DIGITAL VLSI DESIGN



Gary K. Yeap

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Arpita Patel, Jigar Sarda



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Practical Low Power Digital VLSI Design Gary K. Yeap, 2012-12-06 Practical Low Power Digital VLSI Design emphasizes the optimization and trade off techniques that involve power dissipation in the hope that the readers are better prepared the next time they are presented with a low power design problem The book highlights the basic principles methodologies and techniques that are common to most CMOS digital designs The advantages and disadvantages of a particular low power technique are discussed Besides the classical area performance trade off the impact to design cycle time complexity risk testability and reusability are discussed The wide impacts to all aspects of design are what make low power problems challenging and interesting Heavy emphasis is given to top down structured design style with occasional coverage in the semicustom design methodology The examples and design techniques cited have been known to be applied to production scale designs or laboratory settings The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit logic architecture and system Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels Low power techniques are presented at the circuit logic architecture and system levels Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design **Practical Low Power Digital Vlsi Design** Yeap Gary, 2008-12-01

Low Power VLSI Design and Technology Gary K. Yeap, Farid N. Najm, 1996 Low power and low energy VLSI has become an important issue in today's consumer electronics This book is a collection of pioneering applied research papers in low power VLSI design and technology A comprehensive introductory chapter presents the current status of the industry and academic research in the area of low power VLSI design and technology Other topics cover logic synthesis floorplanning circuit design and analysis from the perspective of low power requirements The readers will have a sampling of some key problems in this area as the low power solutions span the entire spectrum of the design process The book also provides excellent references on up to date research and development issues with practical solution techniques [Practical Low Power Digital VLSI Design](#) Felton Boehm, 2018 [Low-Power Digital VLSI Design](#) Abdellatif Bellaouar, Mohamed Elmasry, 2012-12-06 Low Power Digital VLSI Design Circuits and Systems addresses both process technologies and device modeling Power dissipation in CMOS circuits several practical circuit examples and low power techniques are discussed Low voltage issues for digital CMOS and BiCMOS circuits are emphasized The book also provides an extensive study of advanced CMOS subsystem design A low power design methodology is presented with various power minimization techniques at the circuit logic architecture and algorithm levels Features Low voltage CMOS device modeling technology files design rules

Switching activity concept low power guidelines to engineering practice Pass transistor logic families Power dissipation of I/O circuits Multi and low VT CMOS logic static power reduction circuit techniques State of the art design of low voltage BiCMOS and CMOS circuits Low power techniques in CMOS SRAMS and DRAMS Low power on chip voltage down converter design Numerous advanced CMOS subsystems e.g. adders multipliers data path memories regular structures phase locked loops with several design options trading power delay and area Low power design methodology power estimation techniques Power reduction techniques at the logic architecture and algorithm levels More than 190 circuits explained at the transistor level

Low Power Digital Vlsi Design Circuits and Systems S. RAMAMURTHY.,2018

Low Power Digital VLSI Design Swee Yew Choe,1998

Low Power VLSI Design Angsuman Sarkar,Swapnadip De,Manash Chanda,Chandan Kumar Sarkar,2016-08-08 This book teaches basic and advanced concepts new methodologies and recent developments in VLSI technology with a focus on low power design It provides insight on how to use Tanner Spice Cadence tools Xilinx tools VHDL programming and Synopsis to design simple and complex circuits using latest state of the art technologies Emphasis is placed on fundamental transistor circuit level design concepts

Low Voltage, Low Power VLSI Subsystems Kiat Seng Yeo,Kaushik Roy,2005 Designers developing the low voltage low power chips that enable small portable devices face a very particular set of challenges This monograph details design techniques for the low power circuitry required by the many miniaturized business and consumer products driving the electronics market

New Methodologies for Low-power High-performance Digital VLSI Design ,2000

Low-Power VLSI Circuits and Systems Ajit Pal,2014-11-17 The book provides a comprehensive coverage of different aspects of low power circuit synthesis at various levels of design hierarchy starting from the layout level to the system level For a seamless understanding of the subject basics of MOS circuits has been introduced at transistor gate and circuit level followed by various low power design methodologies such as supply voltage scaling switched capacitance minimization techniques and leakage power minimization approaches The content of this book will prove useful to students researchers as well as practicing engineers

Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar,Suganth Paul,Rajesh Garg,2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of an IC However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs This book presents two techniques aimed at reducing leakage power in digital VLSI ICs The first technique reduces leakage through the selective use of high threshold voltage sleep transistors The second technique reduces leakage by applying the optimal Reverse Body Bias RBB voltage This book also shows readers how to turn the leakage problem into an opportunity through

the use of sub threshold logic **Digital Vlsi Design** Singh Ajay Kumar,2010-06-30 This well organised book provides an in depth coverage of VLSI design engineering which ranges from CMOS logic to physical design automation The book begins with a discussion on the structure and operation of MOS as MOSFET is the basic building block for any VLSI design Then it goes on to explain the various fabrication methods of MOSFET and CMOS implementation and properties of MOS inverter circuit and parasitic parameters and resistances associated with MOSFET which determine and ultimately limit the performance of a digital system Besides it describes design methodology and the concept of the combinational static logic circuits sequential circuit design and CMOS dynamic circuits Finally the book examines semiconductor memory and the importance of adder and multiplier circuits for the VLSI designer Primarily intended as a text for the undergraduate and postgraduate students of Electrical and Electronics Engineering the book would also be of considerable value to designers both beginners and professionals Key Features Provides mathematical derivations for both noise margin and logic voltage Explains all combinational and sequential logics separately Contains a large number of solved and unsolved problems based on issues related to digital VLSI design Low Power VLSI Design Danny Conflitti,2001 **Analog and Digital Vlsi Circuit Design** Saradindu Panda, **Low Power Design and Estimation Techniques for Digital VLSI Circuits** Atila Alvandpour,1998 Top-Down Digital VLSI Design Hubert Kaeslin,2014-12-07 Top Down VLSI Design From Architectures to Gate Level Circuits and FPGAs represents a unique approach to learning digital design Developed from more than 20 years teaching circuit design Doctor Kaeslin s approach follows the natural VLSI design flow and makes circuit design accessible for professionals with a background in systems engineering or digital signal processing It begins with hardware architecture and promotes a system level view first considering the type of intended application and letting that guide your design choices Doctor Kaeslin presents modern considerations for handling circuit complexity throughput and energy efficiency while preserving functionality The book focuses on application specific integrated circuits ASICs which along with FPGAs are increasingly used to develop products with applications in telecommunications IT security biomedical automotive and computer vision industries Topics include field programmable logic algorithms verification modeling hardware synchronous clocking and more Demonstrates a top down approach to digital VLSI design Provides a systematic overview of architecture optimization techniques Features a chapter on field programmable logic devices their technologies and architectures Includes checklists hints and warnings for various design situations Emphasizes design flows that do not overlook important action items and which include alternative options when planning the development of microelectronic circuits **Low Power Dissipation in VLSI Circuits. A Study of Low Power VLSI Design Techniques** Arpita Patel,Jigar Sarda,2023-09-08 Seminar paper from the year 2023 in the subject Engineering Computer Engineering grade A language English abstract This book will discuss contemporary optimization techniques that aims low power dissipation in VLSI circuits Since CMOS technology consumes less power it is a key technology for VLSI circuit design With technologies

reaching the scale of 10 nm static and dynamic power dissipation in CMOS VLSI circuits are major issues Dynamic power dissipation is increased due to requirement of high speed and static power dissipation is at much higher side now a days even compared to dynamic power dissipation due to very high gate leakage current and subthreshold leakage Low power consumption is equally important as speed in many applications since it leads to a reduction in the package cost and extended battery life

Introduction to Low-Power Design in VLSIs Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book

Low-Power CMOS VLSI Circuit Design Kaushik Roy, Sharat Prasad, 2000-02-22 A comprehensive look at the rapidly growing field of low power VLSI design Low power VLSI circuit design is a dynamic research area driven by the growing reliance on battery powered portable computing and wireless communications products In addition it has become critical to the continued progress of high performance and reliable microelectronic systems This self contained volume clearly introduces each topic incorporates dozens of illustrations and concludes chapters with summaries and references VLSI circuit and CAD engineers as well as researchers in universities and industry will find ample information on tools and techniques for design and optimization of low power electronic systems Topics include Fundamentals of power dissipation in microelectronic devices Estimation of power dissipation due to switching short circuit subthreshold leakage and diode leakage currents Design and test of low voltage CMOS circuits Power conscious logic and high level synthesis Low power static RAM architecture Energy recovery techniques Software power estimation and optimization

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