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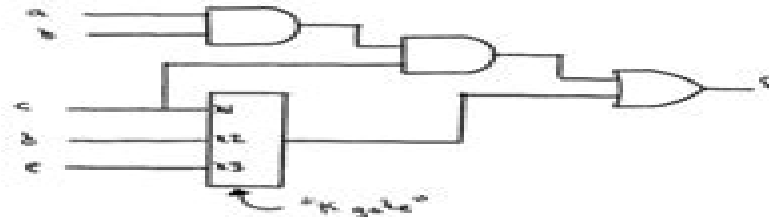
### CSE3017.02 Midterm Exam

Nov. 1, 2017

- Using the rules of logic, show that:  $(a \cdot b) + (\overline{a} \cdot d) = a \cdot (\overline{b} \cdot d)$ . You must show each step and clearly identify each rule used. (Do not use Karnaugh Maps) (10 pts)
- You are given the below circuit. The gate labeled "K gate" has the truth table given below. Your job is to analyze this circuit and come-up with the minimized two-level circuit for the same function that uses only AND, OR and NOT gates. (20 pts)

Truth table for the "K gate":

| X1 | X2 | X3 | F |
|----|----|----|---|
| 0  | 0  | 0  | 1 |
| 0  | 0  | 1  | 0 |
| 0  | 1  | 0  | 1 |
| 0  | 1  | 1  | 0 |
| 1  | 0  | 0  | 1 |
| 1  | 0  | 1  | 0 |
| 1  | 1  | 0  | 1 |
| 1  | 1  | 1  | 0 |



- A temperature sensor has an analog output between 0 and 800 mV. The output voltage 0 means 0 °C and the voltage increases 10 mV for 1 °C increase of temperature. A digital system will use the sensor to set the room temperature between 25-30 °C. The system should control a cooler and an heater in order to set the temperature. a. Choose a proper analog to digital converter in order to digitize the sensor output. Explain each parameter and its effect to the circuit clearly. Hint: choose the parameters carefully; wrong selections can make the design harder. b. Design the combinational circuit that meets the requirements given. Plot the gate level implementation of the circuit. (30 pts)
- Simplify the following function using karnough maps. (10 pts)  
 $F(A,B,C,D) = \Sigma (3,4,12) + d (6,11,14)$
  - Use ONLY NAND gates to implement the F function. (7 pts)
  - Use ONLY NOR gates to implement the F function. (7 pts)
  - Plot the CMOS structure, which has minimum number of transistors to implement F function. (15 pts)
- In class we've designed a half adder and full adder. This time you are going to design half subtractor(subtracts 2 bits) and full subtractor(subtracts 3 bits) with 'Result' and 'Borrow' outputs. Then design a circuit that gives the difference of two 4-bit binary number.(after your design you can show it with blocks)  
 Write Multi-Module Verilog HDL Code.(Create the Half subtractor module, Produce Full subtractor Module with calling Half subtractors then call both of them while you are creating 4-bit subtractor) (25 pts)



**Note:** Please show all your work and write legibly. The use of mobile phones is strictly prohibited. The Calculators, the books and the lecture notes may be used. Duration: 120 mins.

# Digital Design Final Exam And Answers

**RJ Shavelson**



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