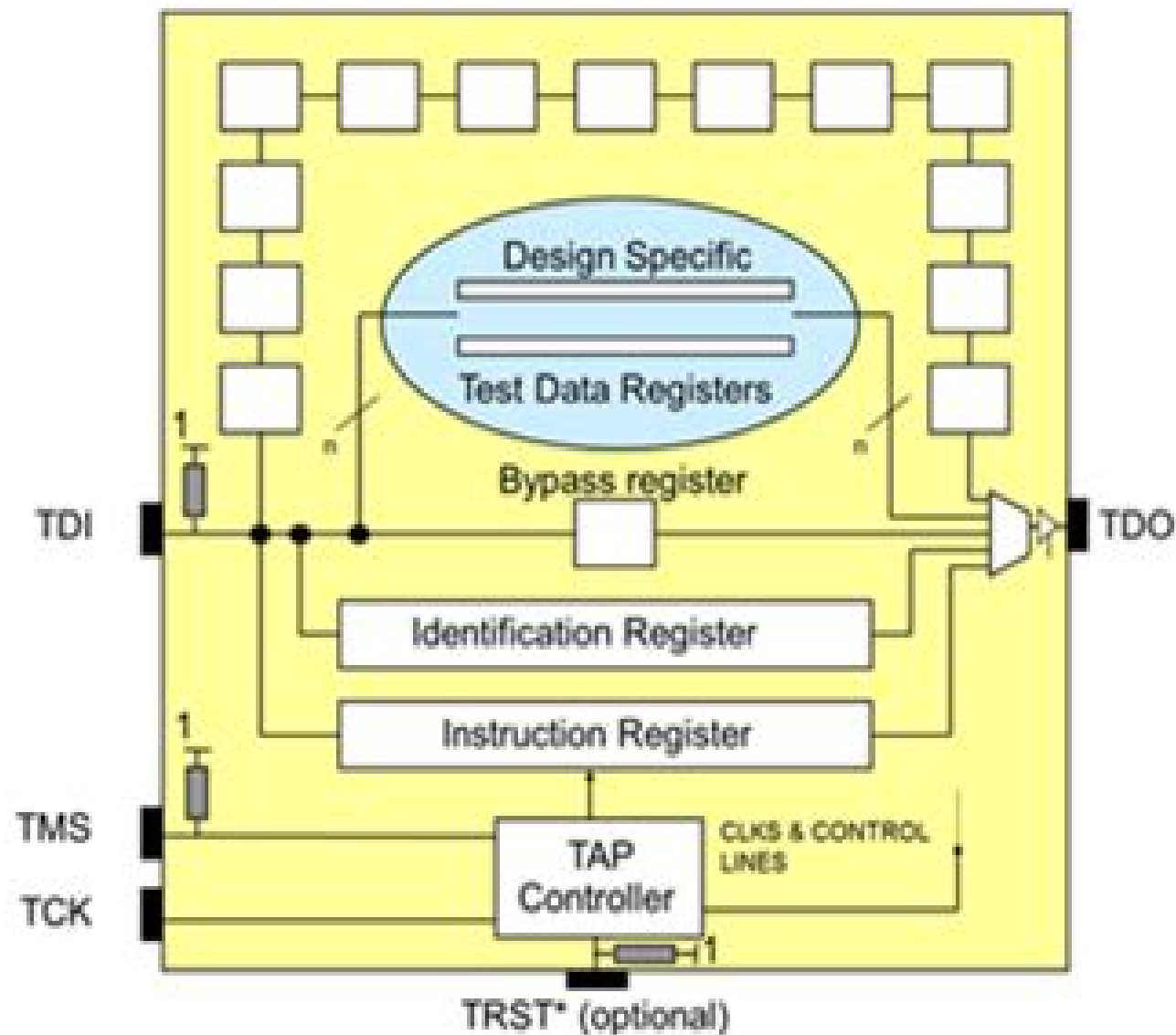


The Boundary-Scan Architecture



Ieee Standard Test Access Port And Boundary Scan

Shasha Hu



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IEEE Standard Test Access Port and Boundary-scan Architecture IEEE Standards Board, IEEE Computer Society. Test Technology Technical Committee, 1990 **IEEE Std 1149.1-2001** ,2001 Circuitry that may be built into an integrated circuit to assist in the test maintenance and support of assembled printed circuit boards is defined The circuitry includes a standard interface through which instructions and test data are communicated A set of test features is defined including a boundary scan register such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards Also a language is defined that slows rigorous description of the component specific aspects of such testability features IEEE Standard Test Access Port and Boundary-scan Architecture ,2001 Circuitry that may be built into an integrated circuit to assist in the test maintenance and support of assembled printed circuit boards is defined The circuitry includes a standard interface through which instructions and test data are communicated A set of test features is defined including a boundary scan register such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards Also a language is defined that slows rigorous description of the component specific aspects of such testability features IEEE Std 1149.1-2001 ,2001 **IEEE Std 1149.1-1990** ,1990 *Elektronische Baugruppen - Aufbau- und Fertigungstechnik - Die Trends von heute - die Chancen von morgen - Vorträge der DVS/GMM-Fachtagung vom 4. bis 5. Februar 2004 in Fellbach* ,2004 *The Boundary-Scan Handbook* Kenneth P. Parker, 2015-11-11 Aimed at electronics industry professionals this 4th edition of the Boundary Scan Handbook describes recent changes to the IEEE1149 1 Standard Test Access Port and Boundary Scan Architecture This updated edition features new chapters on the possible effects of the changes on the work of the practicing test engineers and the new 1149 8 1 standard Anyone needing to understand the basics of boundary scan and its practical industrial implementation will need this book Provides an overview of the recent changes to the 1149 1 standard and the effect of the changes on the work of test engineers Explains the new IEEE 1149 8 1 subsidiary standard and applications Describes the latest updates on the supplementary IEEE testing standards In particular addresses IEEE Std 1149 1 Digital Boundary Scan IEEE Std 1149 4 Analog Boundary Scan IEEE Std 1149 6 Advanced I O Testing IEEE Std 1149 8 1 Passive Component Testing IEEE Std 1149 1 2013 The 2013 Revision of 1149 1 IEEE Std 1532 In System Configuration IEEE Std 1149 6 2015 The 2015 Revision of 1149 6 **Entwurfsmuster** Klaus Quibeldey-Cirkel, 2013-03-07 *Zum Selbsttest von Verbindungsnetzen für Systems on Chip* Markus Rudack, 2007-02-22 Die Entwicklung von Systems on Chip h chstintegrierten Schaltungen die auf einem einzigen Chip vollst ndige elektronische Systeme enthalten wird zunehmend von busbasierten Architekturen dominiert Die Gr nde liegen zum einen in der Wiederverwendung von Teilschaltungen sogenannten IP Cores die ber Busse miteinander kommunizieren und zum anderen in der Notwendigkeit Leitungssysteme hierarchisch anzulegen um eine hohe Leitungsdichte mit geringen Signallaufzeiten auf langen Inter Core Leitungen zu

vereinbaren Lange parallel verlaufende Leitungen wie Busse sind mit zunehmender Strukturverkleinerung und höheren Taktraten von Störeffekten durch Leitungskopplung wie Signalverzerrung und Übersprechen zwischen benachbarten Leitungen betroffen. Inter-Core-Busse stellen daher in Zukunft einen Engpass bei der Leistungsfähigkeit von Core-basierten Systemen dar. Dennoch hat sich noch kein Testverfahren für Inter-Core-Busse etabliert, das Fehler durch Leitungskopplung angemessen erfasst. In dieser Arbeit wird zunächst die Realisierung eines System-on-Chip für die Echtzeitkodierung von Bewegungsbildern hoher Auflösung beschrieben. Dieses System motivierte die Neuentwicklung von Tests auf dynamische Fehler auf Inter-Core-Bussen und von Selbsttestschaltungen für diese Busse. Die neuen Leitungstests basieren auf dem bekannten Walking-1-Test. Sie werden erweitert, um Fehler durch kapazitive und induktive Leitungskopplung zu erfassen. Es werden Schieberegister-basierte Selbsttestrealisierungen dargestellt, die mit minimalem Overhead in den neuen Standard IEEE 1500 für den Test von eingebetteten Cores integriert werden können. Für ein 16-bit-Bussystem wird eine Testschaltung für den Leitungsselbsttest präsentiert, die in einer 0,25-µm-Technologie gefertigt worden ist. Die Auswirkung von Leitungskopplung kann für diese Testschaltung mit einem automatischen Testsystem für digitale Schaltungen gemessen werden. Im Fall von Testsignalen mit ungünstigster Leitungskopplung erreicht die Testschaltung nur etwa die halbe Betriebsfrequenz im Vergleich zum Fall günstigster Leitungskopplung. Dies unterstreicht die Notwendigkeit, Inter-Core-Busse durch einen geeigneten Test auf Kopplungsfehler zu prüfen. Die Messungen weisen eine gute Übereinstimmung mit Simulationen eines RLC-Modell des Bussystems mit nicht linearem Treiber- und Lastmodell auf.

Schlüsselwörter: Leitungstest, Leitungskopplung, System-on-Chip, **Eingebettete Systeme**

Walter Lange, Martin Bogdan, Thomas Schweizer, 2015-10-16. Dieses Buch bietet eine Einführung in die wichtigsten Themen rund um Eingebettete Systeme wie zum Beispiel Technologien, Kommunikation, Mikroprozessoren, Systembeschreibungssprachen, Sensornetzwerke und High-Level-Synthese. Einen breiten Raum nimmt dabei auch das Gebiet der Entwicklungsmethodik ein. Dieser Teil ist besonders für Studenten und Informatiker gedacht, die als Entwickler tätig werden wollen oder es bereits sind. Als eines der ersten deutschsprachigen Lehrbücher schafft es dieses Buch grundlegendes praktisches Wissen über Eingebettete Systeme zu vermitteln. Der Stoff wird anschaulich mit vielen Bildern und Beispielen dargestellt. Auf mathematische Beweise und Formalismen wird dabei bewusst verzichtet. Somit kann der Text auch als Ergänzung für eine formale Behandlung des Themas dienen. Das Werk ist didaktisch entsprechend den Vorlesungen an Hochschulen aufgebaut. Einzelne Kapitel können als getrennte Vorlesungseinheiten verwendet werden.

Eine Technologie für das durchgängige und automatisierte Testen eingebetteter Software Fischer, Till, 2017-07-07. Embedded software demands intensive testing of functional and non-functional requirements. Automation of such tests is performed with different technologies. Source code level tests require specialized unit testing tools. Tests of the high level behavior of control systems follow the model software and hardware in the loop approach. This work studies the integration of such system level and

source code level tests The focus lies on a new programming language to implement test cases

Digital Systems Design with FPGAs and CPLDs Ian Grout, 2011-04-08 Digital Systems Design with FPGAs and CPLDs explains how to design and develop digital electronic systems using programmable logic devices PLDs Totally practical in nature the book features numerous quantify when known case study designs using a variety of Field Programmable Gate Array FPGA and Complex Programmable Logic Devices CPLD for a range of applications from control and instrumentation to semiconductor automatic test equipment Key features include Case studies that provide a walk through of the design process highlighting the trade offs involved Discussion of real world issues such as choice of device pin out power supply power supply decoupling signal integrity for embedding FPGAs within a PCB based design With this book engineers will be able to Use PLD technology to develop digital and mixed signal electronic systems Develop PLD based designs using both schematic capture and VHDL synthesis techniques Interface a PLD to digital and mixed signal systems Undertake complete design exercises from design concept through to the build and test of PLD based electronic hardware This book will be ideal for electronic and computer engineering students taking a practical or Lab based course on digital systems development using PLDs and for engineers in industry looking for concrete advice on developing a digital system using a FPGA or CPLD as its core Case studies that provide a walk through of the design process highlighting the trade offs involved Discussion of real world issues such as choice of device pin out power supply power supply decoupling signal integrity for embedding FPGAs within a PCB based design

DCIS2002 Salvador Bracho del Pino, Mar Martínez, Teresa Riesgo, Miguel Ángel Allende Recio, 2002 Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena Santander en noviembre de 2002 Esta Conferencia ha alcanzado un alto nivel de calidad como consecuencia de su tradición y madurez que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa Desde su origen tiene una gran contribución de Universidades españolas aunque hoy los autores participan desde catorce países

Eingebettete Systeme Oliver Bringmann, Walter Lange, Martin Bogdan, 2018-08-06 Dieses Buch ist eine Einführung in die wichtigsten Themen und Fragestellungen beim Entwurf von Eingebetteten und Cyber Physischen Systemen Ausgehend von den zugrundeliegenden Technologien Prozessor und Netzwerkarchitekturen werden Modellierungssprachen und moderne Ansätze zur Analyse und Synthese von eingebetteten Hardware Software Systemen vorgestellt Einen breiten Raum nimmt das Gebiet Entwicklungsmethodik ein das für Studierende sowie Informatiker und Ingenieure gedacht ist die als Entwickler tätig werden wollen oder es bereits sind Der Stoff wird anschaulich anhand vieler Bilder und Beispiele dargestellt Dabei verzichten wir bewusst auf mathematische Beweise und Formalismen und setzen den Fokus auf die Darstellung aktueller Methoden und Ansätze aus Wissenschaft und Industrie mit hoher Praxisrelevanz Somit kann der Text auch als Ergänzung für eine formale Behandlung des Themas verwendet werden Das Werk orientiert sich didaktisch an einer zweisemestrigen Vorlesung im Masterstudiengang der

Universität Tübingen Einzelne Kapitel können als getrennte Vorlesungseinheiten verwendet werden

Integrated Circuit Test Engineering Ian A. Grout, 2005-12-08 Taking a three pronged approach test engineering from traditional test design and manufacturing view points Integrated Circuit Test Engineering encapsulates the subject as it stands today After introductory background from basic testing rules to trends in technology the reader learns about fabrication processes a complete range of detailed tests and procedures how to design for testability fault simulation automatic test equipment and the economics of testing The text includes Worked examples and exercises well organized references and bibliography An introduction to the use of various software and languages such as MATLAB Spice Verilog HDL and VHDL A series of experiments based on material downloaded from springeronline com showing how to construct a hardware test arrangement for MS Windows PCs This book is a practical tool for advanced undergraduate and graduate electronic engineering students a resource for their tutors and a guide for the practising electronic engineer

Testfreundliche Synthese hochintegrierter Schaltungen Bernhard Eschermann, 2013-03-08

Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1995

Design for AT-Speed Test, Diagnosis and Measurement Benoit Nadeau-Dostie, 2006-04-11 Design for AT Speed Test Diagnosis and Measurement is the first book to offer practical and proven design for testability DFT solutions to chip and system design engineers test engineers and product managers at the silicon level as well as at the board and systems levels Designers will see how the implementation of embedded test enables simplification of silicon debug and system bring up Test engineers will determine how embedded test provides a superior level of at speed test diagnosis and measurement without exceeding the capabilities of their equipment Product managers will learn how the time resources and costs associated with test development manufacture cost and lifecycle maintenance of their products can be significantly reduced by designing embedded test in the product A complete design flow and analysis of the impact of embedded test on a design makes this book a must read before any DFT is attempted

Hochintegrierte Schaltungen: Prüfgerechter Entwurf und Test Hans-Joachim Wunderlich, 2013-03-13 Mit dem vorliegenden Lehrbuch werden erstmalig in deutscher Sprache der prüfgerechte Entwurf und der Test hochintegrierter Schaltungen in umfassender Weise behandelt Das Werk wendet sich an alle die in Studium Lehre Forschung und Entwicklung Kenntnisse auf diesem Gebiet erwerben oder vertiefen möchten Insbesondere erhält der Schaltungsentwickler einen Überblick über die Maßnahmen die zur Verbesserung der Testbarkeit seiner Schaltung beitragen können der Entwickler von Entwurfssystemen findet zahlreiche teilweise neue Algorithmen und Verfahren für den automatisierten Entwurf testbarer Schaltungen und für die zugehörige Testerzeugung Die Verfahren werden in einem einheitlichen theoretischen Rahmen vorgestellt Bei dieser einheitlichen Modellierung der Schaltung und der Algorithmen bleibt jedoch stets die Verbindung zur konkreten technischen Realisierung gewahrt

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now

commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing

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