#### Implementing AVR-like I/O Ports on the AT94K FPGA

#### Features

- . Full Source Code for Input and Output Ports
- Target Implementation Based on AT94K Starter Kit

#### Introduction

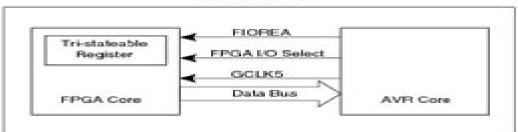
The purpose of this application note is to explain how the FPGA Core of the AT94K Field Programmable System Level Integrated Circuit (FPSLIC\*\*) device can be used to expand the peripherals of the AVR\*\* Core, from two (Port D and Port E) to more peripherals. This application note uses the bi-directional data bus between the two cores of the FPSLIC device.

#### Input Port Description

The Input Port consists of an 8-bit register, which is enabled when the AVR I/O Read Enable (FIOREA) signal and the corresponding FPGA I/O Select are both active. For more information on the AVR I/O Read Enable, please refer to the "AT94K FPSLIC" datasheet, available on the Atmel web site (http://www.atmel.com/atmel/products/prod317.htm). See Figure 1 for further architectural information of the Input Port.

Figure 1. Input Port Block Diagram

#### AT94K Device





Programmable SLI AT94KAL

Application Note

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## **Application Note Atmel**

Jack W. Plunkett



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