.model mmod MODER .model pmod MODE

- 7.5 For the gate shown in Fig. P7.5,
 - Pull-up transistor ratio is 5/5
 - pull-down transistor ratios are 100/5
 - $V_{m} = 1.0 \text{ V}$
 - $\bullet \, \gamma = 0.4 \, \, \mathrm{V}^{\mathrm{to}}$
 - $|2\phi_{\rm c}| = 0.6 \text{ V}$
 - (a) Identify the worst case input combination(s) for V_{oc}
 - (b) Calculate the worst case value of V_{ou} . (Assume that all pull-down transistors have the same body bias and initially, that $V_{ou} = 5\% V_{out}$)

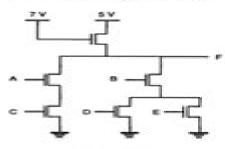


Figure P7.5

SOLUTION:

(a) The worst case input combinations are those that cause only one current path from output to ground. The combinations are listed in the following table.

A=1 $C=1$	B=0
A = 1 $C = 1$	C=0 $E=0$
B=1 $D=1$	A=0 $E=0$
B=1 $D=1$	C=0 $E=0$
B=1 $E=1$	A=0 $D=0$
B=1 $E=1$	C = 0 $D = 0$

(b) The worst case equivalent circuit can be represented by a simple inverter, with the driver W/L=10, load W/L=1. Both transistors are operating is linear region in this case because: Driver: V_{GS} = 5, V_{DS} = 0.25

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Herbert Taub, Donald L. Schilling

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