



Timing Constraints 1/1/2018

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Constraint Type

- ICM Constraints
 - Timing Constraints
 - Clock Domain
 - Setup
 - Hold
 - Frequency
 - Freq
 - Rate
 - Frequency and Phase
 - Launching Conditions
 - **Launch to Launch**
 - Distribution Elements by Name
 - Distribution Elements by Rate
 - By Instance Hierarchy
 - By Clock Edge
 - By Through Ports
 - By Combining Pins
 - By ICM Output
 - Miscellaneous
 - ICM Feedback
 - Time Group Based Area Group
 - Approximate Registers
 - Registers to be Placed in ICMs
 - Path Timing Control

Group Constraints

Item	Constraint	Source
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**Sridhar Gangadharan, Sanjay
Churiwala**



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PLD Based Design with VHDL Vaibbhav Taraate, 2017-01-13 This book covers basic fundamentals of logic design and advanced RTL design concepts using VHDL The book is organized to describe both simple and complex RTL design scenarios using VHDL It gives practical information on the issues in ASIC prototyping using FPGAs design challenges and how to overcome practical issues and concerns It describes how to write an efficient RTL code using VHDL and how to improve the design performance The design guidelines by using VHDL are also explained with the practical examples in this book The book also covers the ALTERA and XILINX FPGA architecture and the design flow for the PLDs The contents of this book will be useful to students researchers and professionals working in hardware design and optimization The book can also be used as a text for graduate and professional development courses

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