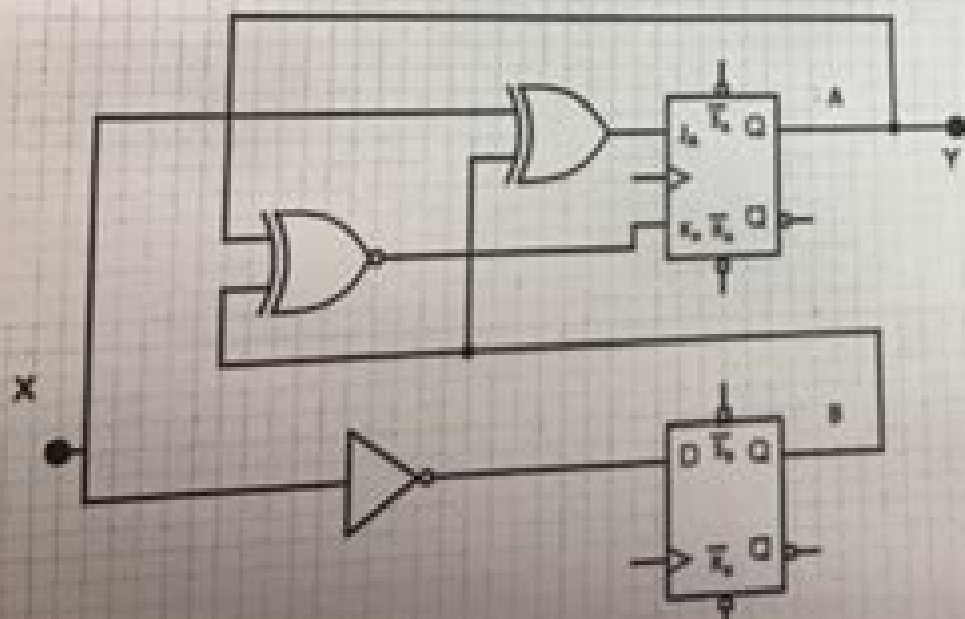


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Problem 5 (25 pts) FSM Circuit Timing Diagram and Re-Design.

- (10 pts) Draw the state transition diagram of the FSM represented by the following circuit.
- (10 pts) Draw the wave forms of A, B, A\*, B\* in following timing diagram for the following circuit.
- (5 pts) Modify the circuit so that the modified circuit would implement the same FSM by replacing the D flip-flop (that produces B) in the circuit by a J-K flip-flop (with inputs J<sub>B</sub> and K<sub>B</sub> and it will also generate B). You need to first write down a truth table to show how J<sub>B</sub> and K<sub>B</sub> depend on X and B, and then write down two Boolean equations of J<sub>B</sub> and K<sub>B</sub> as functions of X and B or just X. You do not need to re-draw the circuit.



# Digital Logic Design Final Exam Solution

**JA Banks**



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## **Table of Contents Digital Logic Design Final Exam Solution**

1. Understanding the eBook Digital Logic Design Final Exam Solution
  - The Rise of Digital Reading Digital Logic Design Final Exam Solution
  - Advantages of eBooks Over Traditional Books
2. Identifying Digital Logic Design Final Exam Solution
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in a Digital Logic Design Final Exam Solution
  - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Logic Design Final Exam Solution
  - Personalized Recommendations
  - Digital Logic Design Final Exam Solution User Reviews and Ratings

- Digital Logic Design Final Exam Solution and Bestseller Lists
- 5. Accessing Digital Logic Design Final Exam Solution Free and Paid eBooks
  - Digital Logic Design Final Exam Solution Public Domain eBooks
  - Digital Logic Design Final Exam Solution eBook Subscription Services
  - Digital Logic Design Final Exam Solution Budget-Friendly Options
- 6. Navigating Digital Logic Design Final Exam Solution eBook Formats
  - ePub, PDF, MOBI, and More
  - Digital Logic Design Final Exam Solution Compatibility with Devices
  - Digital Logic Design Final Exam Solution Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Digital Logic Design Final Exam Solution
  - Highlighting and Note-Taking Digital Logic Design Final Exam Solution
  - Interactive Elements Digital Logic Design Final Exam Solution
- 8. Staying Engaged with Digital Logic Design Final Exam Solution
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Digital Logic Design Final Exam Solution
- 9. Balancing eBooks and Physical Books Digital Logic Design Final Exam Solution
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Digital Logic Design Final Exam Solution
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Logic Design Final Exam Solution
  - Setting Reading Goals Digital Logic Design Final Exam Solution
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Logic Design Final Exam Solution
  - Fact-Checking eBook Content of Digital Logic Design Final Exam Solution
  - Distinguishing Credible Sources

13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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