FET PRINCIPLES AND CIRCUITS

Part 1

Field–Effect Transistors

by Ray Marston

Ray Marston explains FET (Field-Effect Transistor) basics in this opening episode of this new four-part series.

Field-Effect Transistors (FETs) are unipolar devices, and have two big advantages over bipolar transistors: one is that they have a near-infinite input resistance and thus offer near-infinite current and power gain; the other is that their switching action is not marred by charge-storage problems, and they thus outperform most bipolars in terms of digital switching speeds.

Several different basic types of FETs are available, and this opening episode looks at their basic operating principles. Parts 2 to 4 of the series will show practical ways of using FETs.

FET BASICS

An FET is a three-terminal amplifying device. Its terminals are known as the source, gate, and drain, and correspond respectively to the emitter, base, and collector of a normal transistor. Two distinct families of FETs are in general use. The first of these is known as 'junction-gate' types of FETs; this term generally being abbreviated to either JUGFET or (more usually) JFET.

The second family is known as either 'insulated-gate' FETs or Metal Oxide Semiconductor FETs, and these terms are generally abbreviated to IGFET or MOSFET, respectively. 'N-channel' and 'p-channel' versions of both types of FET are available, just as normal transistors are available in npn and pnp versions. Figure 1 shows the symbols and supply polarities of both types of bipolar transistor, and compares them with both JFET versions.

Figure 2 illustrates the basic construction and operating principles of a simple n-channel JFET. It consists of a bar of n-type semiconductor mate-
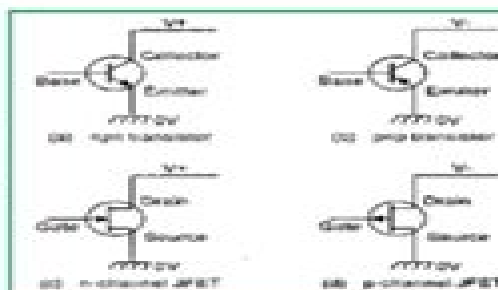
rial with a drain terminal at one end and a source terminal at the other. A p-type control electrode or gate surrounds (and is joined to the surface of) the middle section of the n-type bar, thus forming a p-n junction.

In normal use, the drain terminal is connected to a positive supply and the gate is biased at a value that is negative (or equal) to the source voltage, thus reverse-biasing the JFET's internal p-n junction, and accounting for its very high input impedance.

With zero gate bias applied, a current flow from drain to source via a conductive 'channel' in the n-type bar is formed. When negative gate bias is applied, a high resistance region is formed within the junction, and reduces the width of the n-type conduction channel and, thus reduces the magnitude of the drain-to-source current. As the gate bias is increased, the 'depletion' region spreads deeper into the n-type channel, until eventually, at some 'pinch-off' voltage value, the depletion layer

becomes so deep that conduction ceases.

Thus, the basic JFET of Figure 2 passes maximum current when its gate bias is zero, and its current is reduced or 'depleted' when the gate bias is increased. It is thus known as a 'depletion-type' n-channel JFET. A p-channel version of the device can (in principle) be made by simply transposing the p and n materials.

JFET DETAILS

Figure 3 shows the basic form of construction of a practical n-channel JFET; a p-channel JFET can be made by transposing the p and n materials. All JFETs operate in the depletion mode, as already described. Figure 4 shows the typical transfer characteristics of a low-power n-channel JFET, and illustrates some important features of this type of device. The most important characteristics of the JFET are as follows:

(1). When a JFET is connected to a supply with the polarity shown in Figure 1 (drain +ve for

an n-channel FET, -ve for a p-channel FET), a drain current (I_D) flows and can be controlled via a gate-to-source bias voltage V_{GS}.

(2). I_D is greatest when $V_{GS} = 0$, and is reduced by applying a reverse bias to the gate (negative bias in an n-channel device, positive bias in a p-type). The magnitude of V_{GS} needed to reduce I_D to zero is called the 'pinch-off' voltage, V_P, and typically has a value between 2 and 10 volts. The magnitude of I_D when $V_{GS} = 0$ is denoted I_{DSS}, and typically has a value in the range 2 to 20mA.

(3). The JFET's gate-to-source junction has the characteristics of a silicon diode. When reverse-biased, gate leakage currents (I_{GSS}) are only a couple of nA (1nA = .001µA) at room temperature. Actual gate signal currents are only a fraction of an nA, and the input impedance of the gate is typically thousands of megohms at low frequencies. The gate junction is shunted by a few pF, so the input impedance falls as frequency rises.

If the JFET's gate-to-source junction is forward-biased, it conducts like a normal silicon diode. If it is excessively reverse-biased, it

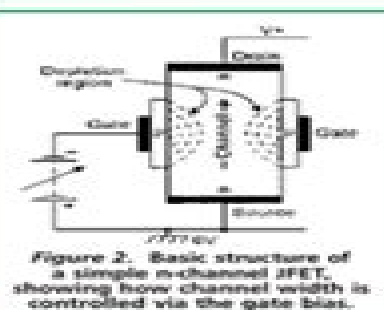**Figure 1.** Comparison of transistor and JFET symbols, notations, and supply polarities.

Figure 2. Basic structure of a simple n-channel JFET, showing how channel width is controlled via the gate bias.

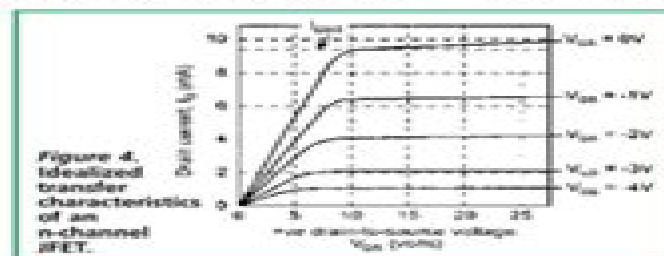**Figure 3.** Construction of n-channel JFET.

Figure 4. Idealized transfer characteristics of an n-channel JFET.
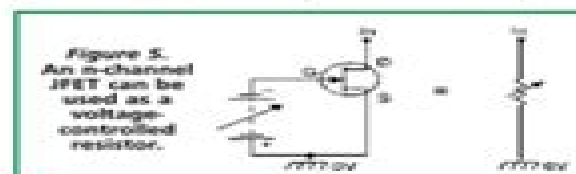
Figure 5. An n-channel JFET can be used as a voltage-controlled resistor.

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