

```
.model nmos NMOS
.model pmos PMOS
```

7.5

For the gate shown in Fig. P7.5,

- Pull-up transistor ratio is 5/5
- pull-down transistor ratios are 100/5
- $V_{th} = 1.0$ V
- $\gamma = 0.4$ V^{1/2}
- $|2\phi_F| = 0.6$ V

- (a) Identify the worst case input combination(s) for V_{OL} .
- (b) Calculate the worst case value of V_{OL} . (Assume that all pull-down transistors have the same body bias and initially, that $V_{OL} = 5\% V_{DD}$.)

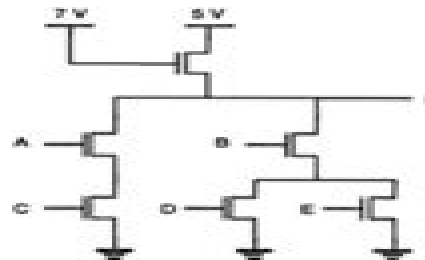


Figure P7.5

SOLUTION:

- (a) The worst case input combinations are those that cause only one current path from output to ground. The combinations are listed in the following table.

$A = 1$	$C = 1$	$B = 0$	
$A = 1$	$C = 1$	$C = 0$	$E = 0$
$B = 1$	$D = 1$	$A = 0$	$E = 0$
$B = 1$	$D = 1$	$C = 0$	$E = 0$
$B = 1$	$E = 1$	$A = 0$	$D = 0$
$B = 1$	$E = 1$	$C = 0$	$D = 0$

- (b) The worst case equivalent circuit can be represented by a simple inverter, with the driver $W/L=10$, load $W/L=1$. Both transistors are operating in linear region in this case because:
- Driver: $V_{GS} = 5$, $V_{DS} = 0.25$

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Solutions Manual Kang, 1995-08-01 *Solutions Manual for An Introduction to Digital and Analog Integrated Circuits and Applications* Sanjit K. Mitra, Sanjit Kumar Mitra, 1981 *Analysis and Design of Digital Integrated Circuits* David A. Hodges, Horace G. Jackson, 1988 This is a state of the art treatment of the circuit design of digital integrated circuits It includes coverage of the basic concepts of static characteristics voltage transfer characteristics noise margins fanout power dissipation and dynamic characteristics propagation delay times and the interrelationships among these parameters The authors are regarded as leading authorities in integrated circuits and MOS technology

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