SECOND EDITION

DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE

JAN M. RABAEY ANANTHA CHANDRAKASAN BORIVOJE NIKOLIĆ

Unique in approach, this text offers comprehensive coverage of new design methodologies and implementation strategies of digital ICs and brings to the forefront a number of new issues that impact the reliability, cost, performance, and power dissipation of chips now reaching the 100-nm realm. This means increased importance in circuit design of deep submicron transistor effects, interconnect, signal integrity, high-performance and low-power design, timing and clock distribution. In contrast to the first edition, the present text focuses entirely on CMOS ICs. While introducing these changes, the text preserves the spirit and goals of the first edition—that is, it successfully bridges the gap between the circuit and system visions on digital design.

Beginning with solid discussions on the operation of electronic devices and in depth analysis of the nucleus of digital design—the inverter—the text gradually channels this knowledge into the design of more complex modules such as gates, controllers, adders, multipliers, and memories. Actual design examples and layouts are interspersed throughout the text. Besides numerous examples, each chapter also contains a number of problems or brain teasers that provoke thinking and understanding while reading. Fully worked-out design problems are available from the web site.

(http://bwrc.eecs.berkeley.edu/icBook)

The text is intended for use in digital circuit design courses conducted for undergraduate and postgraduate students of electronics.



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Books in Print, 1994

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design aids and insight aids to each The rst designer task targeted is global robust sizing This task is supported by a design tool that does automated globally reliable variation aware s ing SANGRIA and an insight aiding tool that extracts designer interpretable whitebox models that relate sizings to circuit performance CAFFEINE SANGRIA searches on several levels of problem dif culty simultaneously from lower cheap to evaluate exploration layers to higher full evaluation exploitation layers structural homotopy SANGRIAmakes maximal use of circuit simulations by performing scalable data mining on simulation results to choose new candidate designs CAFFEINE accomplishes its task by tre ing function induction as a tree search problem It constrains its tree search space via a canonical functional form grammar and searches the space with grammatically constrained genetic programming The second designer task is topology selection topology design Topology selection tools must consider a broad variety of topologies such that an app priate topology is selected must easily adapt to new semiconductor process nodes and readily incorporate new topologies Topology design tools must allow designers to creatively explore new topology ideas as rapidly as possible

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