

Constraining Designs for Synthesis and Timing Analysis: A Practical Guide to Synopsys Design Constraints (SDC)

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Elnora Moreshead

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Constraining Designs for Synthesis and Timing Analysis Sridhar Gangadharan, Sanjay Churiwala, 2014-07-08 This book serves as a hands on guide to timing constraints in integrated circuit design Readers will learn to maximize performance of their IC designs by specifying timing requirements correctly Coverage includes key aspects of the design flow impacted by timing constraints including synthesis static timing analysis and placement and routing Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow all within the context of Synopsys Design Constraints SDC the industry leading format for specifying constraints

Synopsys Design

Constraints Elnora Moreshead, 2021-05-03 Are you have a problem with Synopsys Design Constraints SDC or Altera Timing Analyzer This book will have all the answers for you It explains about each frequently used SDC command specify timing and other design constraints With Altera time analyzer uses industry standard constraint and analysis methodology to report on all data required times data arrival times and clock arrival times for all register to register

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