THIRD EDITION

Fundamentals of
Modern
VLSI Devices

Yuan Taur and Tak H. Ning
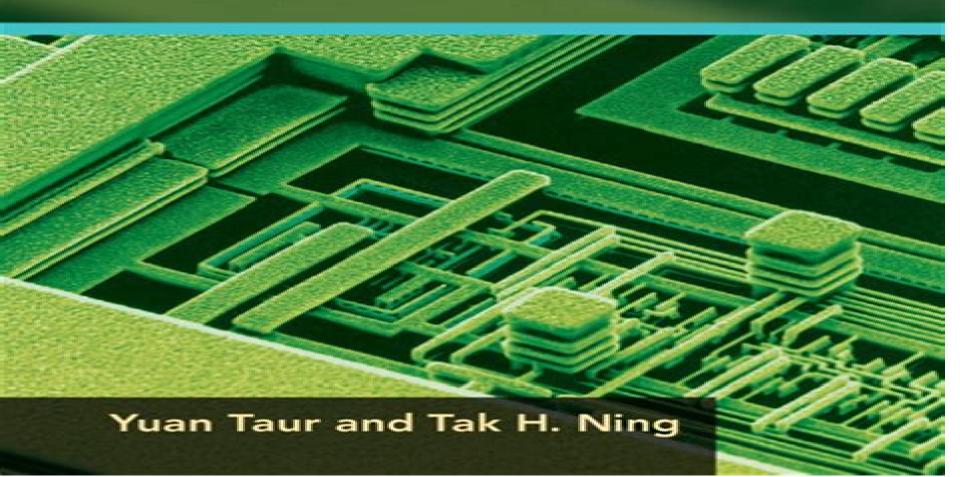
Fundamentals Of Modern Vlsi Devices

Yuan Taur,Tak H. Ning

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   Fundamentals of Modern VLSI Devices Yuan Taur,Tak H. Ning,2021-12-02 A thoroughly updated third edition of an classic and widely adopted text perfect for practical transistor design and in the classroom Covering a variety of recent developments the internationally renowned authors discuss in detail the basic properties and designs of modern VLSI devices as well as factors affecting performance Containing around 25% new material coverage has been expanded to include high k gate dielectrics metal gate technology strained silicon mobility non GCA Gradual Channel Approximation modelling of MOSFETs short channel FinFETS and symmetric lateral bipolar transistors on SOI Chapters have been reorganized to integrate the appendices into the main text to enable a smoother learning experience and numerous additional end of chapter homework exercises 30% are included to engage students with real world problems and test their understanding A perfect text for senior undergraduate and graduate students taking advanced semiconductor devices courses and for practicing silicon device professionals in the semiconductor industry   **Fundamentals Of Modern Vlsi Devices** Yuan Taur,Tak H. Ning,2004-10-01 This book examines in detail the basic properties and design including chip integration of CMOS and bipolar VLSI devices and discusses the various factors that affect their performance The authors begin with a thorough review of the relevant aspects of semiconductor physics and proceed to a description of the design of CMOS and bipolar devices The optimization of these devices for VLSI applications is also covered The authors highlight the intricate interdependencies and subtle trade offs between those device parameters such as power consumption and packing density that affect circuit performance and manufacturability They also discuss in detail the scaling and physical limits to the scaling of CMOS and bipolar devices The book contains many exercises and can be used as a textbook for senior undergraduate or first year graduate courses on microelectronics or VLSI devices It will also be a valuable reference volume for practising engineers involved in research and development in the electronics industry   **Fundamentals of Modern VLSI Devices International Student Edition** Yuan Taur,Tak H. Ning,2010-06-29   *Nano and Giga Challenges in Microelectronics* J. Greer,A. Korkin,J. Labanowski,2003-10-24 The book is designed as an introduction for engineers and researchers wishing to

obtain a fundamental knowledge and a snapshot in time of the cutting edge in technology research As a natural consequence Nano and Giga Challenges is also an essential reference for the gurus wishing to keep abreast of the latest directions and challenges in microelectronic technology development and future trends The combination of viewpoints presented within the book can help to foster further research and cross disciplinary interaction needed to surmount the barriers facing future generations of technology design Key Features Quickly becoming the hottest topic of the new millennium 2 4 billion dollars funding in US alone Current status and future trends of micro and nanoelectronics research Written by leading experts in the corresponding research areas Excellent tutorial for graduate students and reference for gurus   CMOS R. Jacob Baker,2008 This edition provides an important contemporary view of a wide range of analog digital circuit blocks the BSIM model data converter architectures and more The authors develop design techniques for both long and short channel CMOS technologies and then compare the two   *High Dielectric Constant Materials* Howard Huff,2005 Issues relating to the high K gate dielectric are among the greatest challenges for the evolving International Technology Roadmap for Semiconductors ITRS More than just an historical overview this book will assess previous and present approaches related to scaling the gate dielectric and their impact along with the creative directions and forthcoming challenges that will define the future of gate dielectric scaling technology Topics include an extensive review of Moore s Law the classical regime for SiO2 gate dielectrics the transition to silicon oxynitride gate dielectrics the transition to high K gate dielectrics including the drive towards equivalent oxide thickness in the single digit nanometer regime and future directions and issues for ultimate technology generation scaling The vision wisdom and experience of the team of authors will make this book a timely relevant and interesting resource focusing on fundamentals of the 45 nm Technology Generation and beyond   *Advanced Ultra Low-Power Semiconductor Devices* Shubham Tayal,Abhishek Kumar Upadhyay,Shiromani Balmukund Rahi,Young Suh Song,2023-10-30 ADVANCED ULTRA LOW POWER SEMICONDUCTOR DEVICES Written and edited by a team of experts in the field this important new volume broadly covers the design and applications of metal oxide semiconductor field effect transistors This outstanding new volume offers a comprehensive overview of cutting edge semiconductor components tailored for ultra low power applications These components pivotal to the foundation of electronic devices play a central role in shaping the landscape of electronics With a focus on emerging low power electronic devices and their application across domains like wireless communication biosensing and circuits this book presents an invaluable resource for understanding this dynamic field Bringing together experts and researchers from various facets of the VLSI domain the book addresses the challenges posed by advanced low power devices This collaborative effort aims to propel engineering innovations and refine the practical implementation of these technologies Specific chapters delve into intricate topics such as Tunnel FET negative capacitance FET device circuits and advanced FETs tailored for diverse circuit applications Beyond device centric discussions the book delves into the design intricacies of low power memory systems the fascinating realm of neuromorphic

computing and the pivotal issue of thermal reliability Authors provide a robust foundation in device physics and circuitry while also exploring novel materials and architectures like transistors built on pioneering channel dielectric materials This exploration is driven by the need to achieve both minimal power consumption and ultra fast switching speeds meeting the relentless demands of the semiconductor industry The book s scope encompasses concepts like MOSFET FinFET GAA MOSFET the 5 nm and 7 nm technology nodes NCFET ferroelectric materials subthreshold swing high k materials as well as advanced and emerging materials pivotal for the semiconductor industry s future **Charakterisierung von Leckstrompfaden in DRAM Speicherzellen und deren Reduktion** Andreas Weber,2007 *Werkstofftechnik* Serope Kalpakjian,Steven R. Schmid,Ewald Werner,2011 **Physik der Halbleiterbauelemente** Simon M. Sze,Yiming Li,Kwok K. Ng,2021-10-26 Physik der Halbleiterbauelemente Das Standardwerk zur Physik der Halbleiterbauelemente erstmals auf Deutsch Dieses einzigartige Buch geschrieben von Pionieren auf dem Gebiet behandelt s mtliche Aspekte der Physik der Halbleiterbauelemente die zu deren Verst ndnis Betrieb Weiter und Neuentwicklung notwendig sind Wie das englische Original ist die deutsche Ausgabe ein u erst n tzliches Nachschlagewerk in der industrieorientierten Halbleiterforschung und eignet sich ebenfalls ausgezeichnet als Einstiegsliteratur f r Studierende sowie als Unterrichtsmaterial f r Vortragende Bei der deutschen Ausgabe wurde besonderer Wert auf eine gute Lesbarkeit gelegt und daher die bersetzung teilweise unter R ckgriff auf die von den Autoren zitierten Originalquellen so gestaltet dass unn tige Anglizismen vermieden werden Das englische Fachvokabular ist erg nzend an den entsprechenden Stellen im Text eingearbeitet um den Leserinnen und Lesern den Gebrauch der englischsprachigen Fachliteratur zu erleichtern Gelegentliche Anmerkungen im Text und Verweise auf weitere Originalquellen tragen zus tzlich zum besseren Verst ndnis der Materie bei Als das Referenzwerk schlechthin ist der Sze ein Muss f r alle die sich in Forschung Entwicklung und Lehre mit Halbleiterbauelementen besch ftigen Die Inhalte sind kompakt und pr zise beschrieben und eignen sich perfekt f r den Einstieg in das jeweilige Gebiet komplettiert durch vertiefende bungsbeispiele zu jedem Kapitel Physik der Halbleiterbauelemente bietet eine unerreichte Detailf lle und ausf hrliche Informationen ber die Physik und den Betrieb aller relevanten Halbleiterbauelemente mit 1000 Literaturangaben 650 technischen Illustrationen sowie 25 Tabellen mit Material und Bauelementparametern Aus dem Inhalt Halbleiterphysik Grundlagen p n berg nge Metall Halbleiter Kontakte MIS Kondensatoren Bipolartransistoren MOSFETs Nichtfl chtige Speicher JFETs MESFETs und MODFETs Tunnel Bauelemente IMPATT Dioden TE und RST Devices Thyristoren und Leistungsbauelemente Photodetektoren und Solarzellen Sensoren Device Circuit Co-Design Issues in FETs Shubham Tayal,Billel Smaani,Shiromani Balmukund Rahi,Samir Labiod,Zeinab Ramezani,2023-08-22 This book provides an overview of emerging semiconductor devices and their applications in electronic circuits which form the foundation of electronic devices Device Circuit Co Design Issues in FETs provides readers with a better understanding of the ever growing field of low power electronic devices and their applications in the wireless biosensing and circuit domains The book brings researchers and

engineers from various disciplines of the VLSI domain together to tackle the emerging challenges in the field of engineering and applications of advanced low power devices in an effort to improve the performance of these technologies The chapters examine the challenges and scope of FinFET device circuits 3D FETs and advanced FET for circuit applications The book also discusses low power memory design neuromorphic computing and issues related to thermal reliability The authors provide a good understanding of device physics and circuits and discuss transistors based on the new channel dielectric materials and device architectures to achieve low power dissipation and ultra high switching speeds to fulfill the requirements of the semiconductor industry This book is intended for students researchers and professionals in the field of semiconductor devices and nanodevices as well as those working on device circuit co design issues **Non-logic Devices in Logic Processes** Yanjun Ma,Edwin Kan,2017-03-29 This book shows readers how to design semiconductor devices using the most common and lowest cost logic CMOS processes Readers will benefit from the author s extensive industrial experience and the practical approach he describes for designing efficiently semiconductor devices that typically have to be implemented using specialized processes that are expensive time consuming and low yield The author presents an integrated picture of semiconductor device physics and manufacturing techniques as well as numerous practical examples of device designs that are tried and true **Thermal and Power Management of Integrated Circuits** Arman Vassighi,Manoj Sachdev,2006-06-01 In Thermal and Power Management of Integrated Circuits power and thermal management issues in integrated circuits during normal operating conditions and stress operating conditions are addressed Thermal management in VLSI circuits is becoming an integral part of the design test and manufacturing Proper thermal management is the key to achieve high performance quality and reliability Performance and reliability of integrated circuits are strong functions of the junction temperature A small increase in junction temperature may result in significant reduction in the device lifetime This book reviews the significance of the junction temperature as a reliability measure under nominal and burn in conditions The latest research in the area of electro thermal modeling of integrated circuits will also be presented Recent models and associated CAD tools are covered and various techniques at the circuit and system levels are reviewed Subsequently the authors provide an insight into the concept of thermal runaway and how it may best be avoided A section on low temperature operation of integrated circuits concludes the book **Introduction to Nanoscale Science and Technology** Massimiliano Ventra,Stephane Evoy,James R. Heflin,2006-04-11 Nanoscale science and technology is a young promising field that encompasses a wide range of disciplines including physics chemistry biology electrical engineering chemical engineering and materials science With rapid advances in areas such as molecular electronics synthetic biomolecular motors DNA based self assembly and manipulation of individual atoms nanotechnology has captured the attention and imagination of researchers and the general public Introduction to Nanoscale Science and Technology provides a broad and thorough introduction that is aimed specifically at undergraduate seniors and early graduate students in all of the disciplines enumerated above It will also

be of value to academic industrial and government researchers interested in a primer in the field The book consists of twenty three chapters arranged in seven sections All chapters have been written by experts from each respective field Exercises and general references are provided at the end of each chapter to encourage students to expand on the topics discussed in the book   Simulation and Optimization of Digital Circuits Vazgen Melikyan,2018-04-12 This book describes new fuzzy logic based mathematical apparatus which enable readers to work with continuous variables while implementing whole circuit simulations with speed similar to gate level simulators and accuracy similar to circuit level simulators The author demonstrates newly developed principles of digital integrated circuit simulation and optimization that take into consideration various external and internal destabilizing factors influencing the operation of digital ICs The discussion includes factors including radiation ambient temperature electromagnetic fields and climatic conditions as well as non ideality of interconnects and power rails   **New Prospects of Integrating Low Substrate Temperatures with Scaling-Sustained Device Architectural Innovation** Nabil Shovon Ashraf,Shawon Alam,Mohaiminul Alam,2022-06-01 In order to sustain Moore s Law based device scaling principal attention has focused on toward device architectural innovations for improved device performance as per ITRS projections for technology nodes up to 10 nm Efficient integration of lower substrate temperatures   **Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes** Hsiao-Hsuan Liu,Francky Catthoor,2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area

product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes   Contemporary Trends in Semiconductor Devices Rupam Goswami,Rajesh Saha,2022-02-16 This book covers evolution concept and applications of modern semiconductor devices such as tunnel field effect transistors TFETs vertical super thin body MOSFETs ion sensing FETs ISFETs non conventional solar cells opto electro mechanical devices and thin film transistors TFTs Comprising of theory experimentation and applications of devices the chapters describe state of art methods and techniques which shall be highly assistive in having an overall perspective on emerging technologies and working on a research area The book is aimed at the scholars enthusiasts and researchers who are currently working on devices in the contemporary era of semiconductor devices Additionally the chapters are lucid and descriptive and carry the potential of serving as a reference book for scholars in their undergraduate studies who are looking ahead for a prospective career in semiconductor devices   *Variation-Aware Advanced CMOS Devices and SRAM* Changhwan Shin,2016-06-06 This book provides a comprehensive overview of contemporary issues in complementary metal oxide semiconductor CMOS device design describing how to overcome process induced random variations such as line edge roughness random dopant fluctuation and work function variation and the applications of novel CMOS devices to cache memory or Static Random Access Memory SRAM The author places emphasis on the physical understanding of process induced random variation as well as the introduction of novel CMOS device structures and their application to SRAM The book outlines the technical predicament facing state of the art CMOS technology development due to the effect of ever increasing process induced random intrinsic variation in transistor performance at the sub 30 nm technology nodes Therefore the physical understanding of process induced random intrinsic variations and the technical solutions to address these issues plays a key role in new CMOS technology development This book aims to provide the reader with a deep understanding of the major random variation sources and the characterization of each random variation source Furthermore the book presents various CMOS device designs to surmount the random variation in future CMOS technology emphasizing the applications to SRAM

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