



(b)

```

module sort (Clock, Resetcn, s, Wrlnit, Rd, DataIn, RAdd, DataOut, Done);
  parameter n = 4;
  input Clock, Resetcn, s, Wrlnit, Rd;
  input [n-1:0] DataIn;
  input [1:0] RAdd;
  output [n-1:0] DataOut;
  output Done;
  wire [0:3] Ci, Cj, Cmux;
  reg [1:0] Imax;
  wire [n-1:0] R0, R1, R2, R3, A, B;
  wire [n-1:0] RData, ABMux;
  wire BltA, zi, zj;
  reg Int, Csel, Wr, Ain, Bin, Aout, Bout, LI, LJ, EI, EJ, Done;
  reg [3:0] y, Y;
  reg Rin0, Rin1, Rin2, Rin3;
  reg [n-1:0] ABData;
  wire [0:3] Rout, ExtAdd;
  wire [0:3] Addr0; //Parallel load for Ci

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