LVDS SERDES Transmitter/Receiver IP Cores User Guide

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The low-voltage differential signaling serializer or descrializer (LVDS SERDES) IP cores (ALTLVDS_TX and ALTLVDS_RX) implement the LVDS SERDES interfaces to transmit and receive high-speed differential data. You can configure the features of these IP cores using the IP Catalog and parameter editor.

Related Information

LVDS SERDES Transmitter/Receiver IP Cores User Guide Archives on page 68 Provides a list of user guides for previous versions of the ALTLVDS_TX and ALTLVDS_RX IP cores.

Features

Table 1: ALTLVDS_TX and ALTLVDS_RX Features

This table lists the features of the ALTLVDS_TX and ALTLVDS_RX IP cores.

Note: The ALTLVDS_TX and ALTLVDS_RX IP cores are not available for the Stratix* 10 and Arria* 10 device families. For Stratix 10 and Arria 10 devices, use the Altera LVDS SERDES IP core.

IP Core	Features	Supported devices
ALTLVDS_ TX and ALTLVDS_ RX	Parameterizable data channel widths	All Stratix, Arria, and Cyclone ^a series devices.
	Parameterizable serializer/deserializer (SERDES) factors	
	Registered input and output ports	
	Support for external phase-locked loops (PLL)	
	PLLs sharing between transmitters and receivers	
	PLL control signals	
ALTLVDS_ RX Only	Dynamic phase alignment (DPA) mode support(1)	All Stratix and Arria series devices.
	Soft clock data recovery (CDR) mode support ^{CD}	
	DPA PLL calibration support(1)	All Stratix series devices.

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⁽¹⁾ DPA is available starting from Stratix GX onwards. The first generation Stratix device family does not support DPA.

⁽²⁾ CDR is not available in the first generation Stratix device family and the Stratix II device family. However, soft-CDR is available in all other Stratix series including Stratix GX and Stratix II GX...

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Feng Zhang

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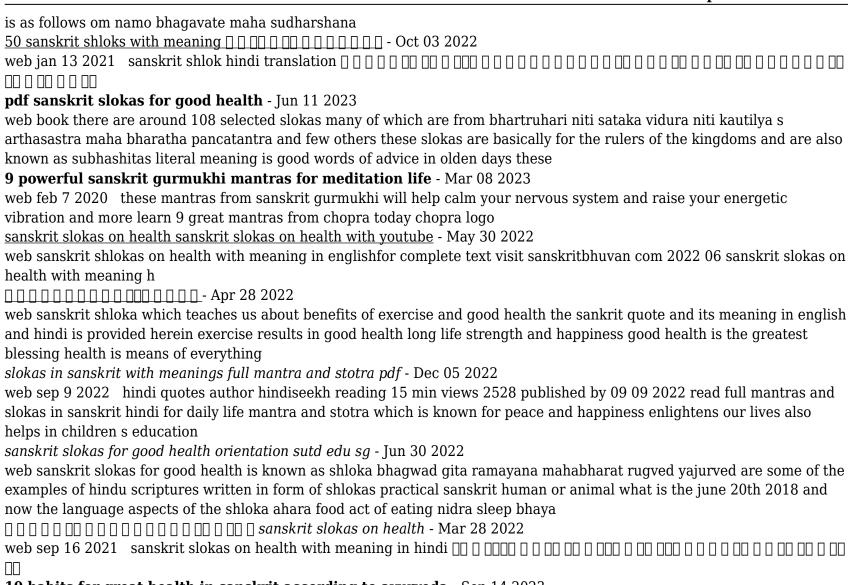
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