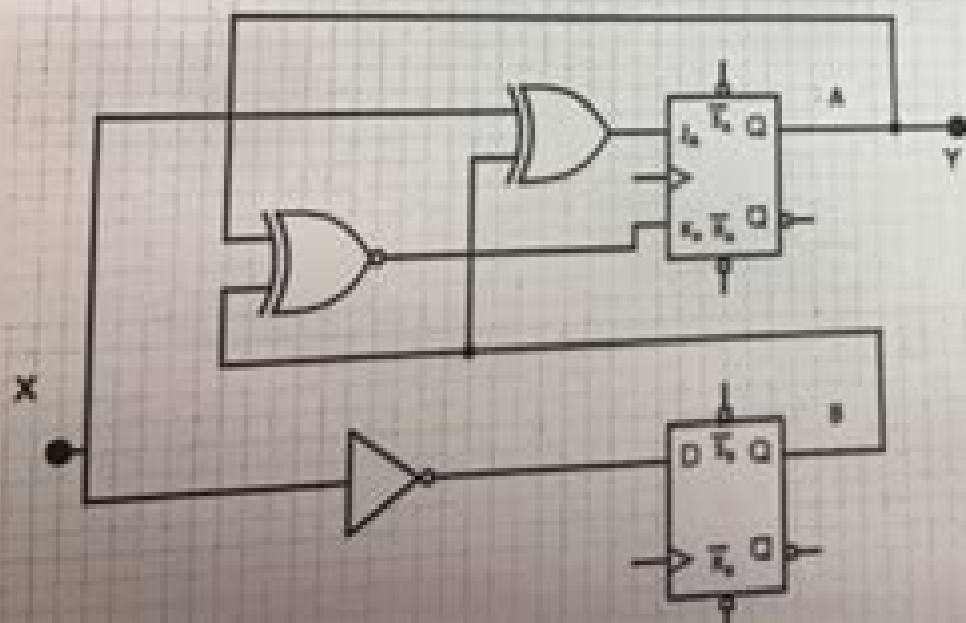


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Problem 5 (25 pts) FSM Circuit Timing Diagram and Re-Design.

- (10 pts) Draw the state transition diagram of the FSM represented by the following circuit.
- (10 pts) Draw the wave forms of A , B , A^* , B^* in following timing diagram for the following circuit.
- (5 pts) Modify the circuit so that the modified circuit would implement the same FSM by replacing the D flip-flop (that produces B) in the circuit by a J-K flip-flop (with inputs J_B and K_B and it will also generate B). You need to first write down a truth table to show how J_B and K_B depend on X and B , and then write down two Boolean equations of J_B and K_B as functions of X and B or just X . You do not need to re-draw the circuit.



Digital Logic Design Final Exam Solution

Arshad Iqbal



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12 Gallium Arsenide Digital Circuits Questions Chapter 13 Introduction to Digital Electronics Questions Chapter 14 Latches and Flip Flops Questions Chapter 15 MOS Digital Circuits Questions Chapter 16 Multivibrators Circuits Questions Chapter 17 Number Systems Questions Chapter 18 Pass Transistor Logic Circuits Questions Chapter 19 Pseudo NMOS Logic Circuits Questions Chapter 20 Random Access Memory Cells Questions Chapter 21 Read Only Memory ROM Questions Chapter 22 Semiconductor Memories Questions Chapter 23 Sense Amplifiers and Address Decoders Questions Chapter 24 SPICE Simulator Questions Chapter 25 Transistor Transistor Logic TTL Questions The Analog to Digital Converters Quiz Questions PDF e Book Chapter 1 interview questions and answers on Digital to analog converter and seven segment display The BICMOS Digital Circuits Quiz Questions PDF e Book Chapter 2 interview questions and answers on Introduction to BICMOS BICMOS inverter and dynamic operation The Bipolar Junction Transistors Quiz Questions PDF e Book Chapter 3 interview questions and answers on Basic transistor operation collector characteristic curves current and voltage analysis DC load line derating PD maximum maximum transistor rating transistor as amplifier transistor characteristics and parameters transistor regions transistor structure transistors and switches The BJT Advanced Technology Dynamic Switching Quiz Questions PDF e Book Chapter 4 interview questions and answers on Saturating and non saturating logic and transistor switching times The BJT Digital Circuits Quiz Questions PDF e Book Chapter 5 interview questions and answers on BJT inverters Diode Transistor Logic DTL Resistor Transistor Logic RTL and RTL SR flip flop The CMOS Inverters Quiz Questions PDF e Book Chapter 6 interview questions and answers on Circuit structure CMOS dynamic operation CMOS dynamic power dissipation CMOS noise margin and CMOS static operation The CMOS Logic Gates Circuits Quiz Questions PDF e Book Chapter 7 interview questions and answers on Basic CMOS gate structure basic CMOS gate structure representation CMOS exclusive OR gate CMOS NAND gate CMOS NOR gate complex gate PUN PDN from PDN PUN and transistor sizing The Digital Logic Gates Quiz Questions PDF e Book Chapter 8 interview questions and answers on NAND NOR and NXOR gates applications of gate building gates from gates electronics and gate electronics OR gate gate basics gates with more than two inputs masking in logic gates negation OR and XOR gates The Dynamic Logic Circuits Quiz Questions PDF e Book Chapter 9 interview questions and answers on Cascading dynamic logic gates domino CMOS logic dynamic logic circuit leakage effects dynamic logic circuits basic principle dynamic logic circuits charge sharing and dynamic logic circuits noise margins The Emitter Coupled Logic ECL Quiz Questions PDF e Book Chapter 10 interview questions and answers on Basic gate circuit ECL basic principle ECL families ECL manufacturer specification electronics and speed electronics power dissipation fan out signal transmission thermal effect and wired capability The Encoders and Decoders Quiz Questions PDF e Book Chapter 11 interview questions and answers on Counter decoder applications decoder basics decoding and encoding encoder applications encoder basics The Gallium Arsenide Digital Circuits Quiz Questions PDF e Book Chapter 12 interview questions and answers on Buffered FET logic DCFL disadvantages GAAS DCFL basics gallium arsenide basics logic gates using

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Table of Contents Digital Logic Design Final Exam Solution

1. Understanding the eBook Digital Logic Design Final Exam Solution
 - The Rise of Digital Reading Digital Logic Design Final Exam Solution
 - Advantages of eBooks Over Traditional Books
2. Identifying Digital Logic Design Final Exam Solution
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in a Digital Logic Design Final Exam Solution
 - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Logic Design Final Exam Solution
 - Personalized Recommendations
 - Digital Logic Design Final Exam Solution User Reviews and Ratings
 - Digital Logic Design Final Exam Solution and Bestseller Lists
5. Accessing Digital Logic Design Final Exam Solution Free and Paid eBooks
 - Digital Logic Design Final Exam Solution Public Domain eBooks
 - Digital Logic Design Final Exam Solution eBook Subscription Services
 - Digital Logic Design Final Exam Solution Budget-Friendly Options
6. Navigating Digital Logic Design Final Exam Solution eBook Formats
 - ePub, PDF, MOBI, and More
 - Digital Logic Design Final Exam Solution Compatibility with Devices
 - Digital Logic Design Final Exam Solution Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Digital Logic Design Final Exam Solution
 - Highlighting and Note-Taking Digital Logic Design Final Exam Solution
 - Interactive Elements Digital Logic Design Final Exam Solution

8. Staying Engaged with Digital Logic Design Final Exam Solution
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Logic Design Final Exam Solution
9. Balancing eBooks and Physical Books Digital Logic Design Final Exam Solution
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Digital Logic Design Final Exam Solution
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Digital Logic Design Final Exam Solution
 - Setting Reading Goals Digital Logic Design Final Exam Solution
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Digital Logic Design Final Exam Solution
 - Fact-Checking eBook Content of Digital Logic Design Final Exam Solution
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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~~philippine mechanical engineering laws and code~~

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